

SANYO

No.2622B

L78LR05**150mA, 5V 5-Pin Voltage Regulator
with Reset Function****Overview**

The L78LR05 is a voltage regulator IC that performs the reset signal generating function when the power supply of a microcomputer system is turned ON/OFF. The L78LR05 is convenient for battery backup system at the time of power failure. The reset threshold voltage V_{RT} is ranked as shown below.

V_{RT} rank	B	C	D	E	F	G	H
V_{RT} (V)	4.8	4.5	4.2	3.9	3.6	3.3	3.0

Applications

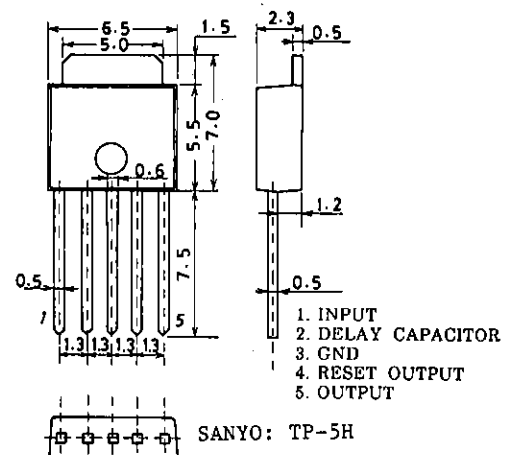
- Prevention of malfunction that may occur when the power supply of a microcomputer is turned ON/OFF.
- Measures taken against abnormal operations that may occur at the time of instantaneous break of power supply
- Direct battery backup for SRAM

Features

- 5V, 150mA output
- Capable of generating a microcomputer reset signal
- No battery-regulator switching circuit required at the battery backup mode (Output leakage current: $2\mu\text{A}$ or less)
- An external capacitor can be used to set the reset output delay time.
- Applicable to the power supply of CMOS, NMOS microcomputers
- Especially suited for use as an on-board regulator for a microcomputer system
- Small-sized power package TP-5H permitting the equipment to be made compact
- The allowable power dissipation can be increased by being surface-mounted on the board.
- Capable of being mounted in a variety of methods because of various lead forming versions available
- On-chip protectors (overcurrent limiter, ASO protector, thermal protector)

Package Dimensions
(unit: mm)

3103



L78LR05

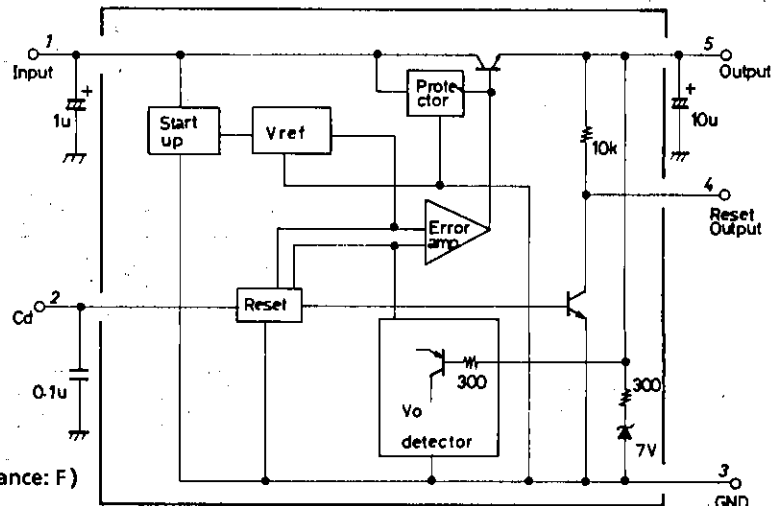
Maximum Ratings at $T_a = 25^\circ\text{C}$				unit
Maximum Input Voltage	$V_{IN \text{ max}}$		25	V
Allowable Power Dissipation	$P_d \text{ max}$	(No fin)	1.0	W
Operating Temperature	T_{op}		-30 to +80	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$				unit
Input Voltage	V_{IN}		7.5 to 20	V
Output Current	I_{OUT}		1 to 150	mA

Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{IN} = 10\text{V}$, $I_{OUT} = 40\text{mA}$, $c_{in} = 1\mu\text{F}$, $c_o = 10\mu\text{F}$

			min	typ	max	unit	
Output Voltage	V_{OUT1}	$T_j = 25^\circ\text{C}$	4.8	5.0	5.2	V	
	V_{OUT2}	$7\text{V} \leq V_{IN} \leq 20\text{V}$, $1\text{mA} \leq I_{OUT} \leq 70\text{mA}$	4.75		5.25	V	
Line Regulation	$\Delta V_{o \text{ LINE1}}$	$T_j = 25^\circ\text{C}$, $7\text{V} \leq V_{IN} \leq 20\text{V}$		6.0	75	mV	
	$\Delta V_{o \text{ LINE2}}$	$T_j = 25^\circ\text{C}$, $8\text{V} \leq V_{IN} \leq 20\text{V}$		3.0	50	mV	
Load Regulation	$\Delta V_{o \text{ LOAD1}}$	$T_j = 25^\circ\text{C}$, $1\text{mA} \leq I_{OUT} \leq 100\text{mA}$		9.0	60	mV	
	$\Delta V_{o \text{ LOAD2}}$	$T_j = 25^\circ\text{C}$, $1\text{mA} \leq I_{OUT} \leq 40\text{mA}$		3.0	30	mV	
Current Dissipation	I_{CC}	$T_j = 25^\circ\text{C}$, $I_{OUT} = 100\text{mA}$		1.4	3.4	mA	
Current Dissipation Variation	$\Delta I_{CC \text{ LINE}}$	$8\text{V} \leq V_{IN} \leq 20\text{V}$		0.12	1.5	mA	
	$\Delta I_{CC \text{ LOAD}}$	$1\text{mA} \leq I_{OUT} \leq 40\text{mA}$		0.01	0.1	mA	
Output Noise Voltage	V_{NO}	$10\text{Hz} \leq f \leq 100\text{kHz}$, $I_o = 1\text{mA}$		80		μV	
Temperature Coefficient of Output Voltage	$\Delta V_{OUT}/\Delta T_j$	$I_{OUT} = 1\text{mA}$, $T_j = 25 \text{ to } 125^\circ\text{C}$		± 0.5		$\text{mV}/^\circ\text{C}$	
Ripple Rejection	R_{rej}	$T_j = 25^\circ\text{C}$, $f = 120\text{Hz}$, $8\text{V} \leq V_{IN} \leq 18\text{V}$		79		dB	
Dropout Voltage	V_{DROP}	$T_j = 25^\circ\text{C}$		1.5	2.2	V	
Output Short Current	I_{OSC}	$T_j = 25^\circ\text{C}$	150	300	450	mA	
"H"-Reset Output Voltage	V_{ORH}	$T_j = 25^\circ\text{C}$	4.8	5.0	5.2	V	
"L"-Reset Output Voltage	V_{ORL}	$T_j = 25^\circ\text{C}$, $V_{IN} = 3\text{V}$, $I_o = 1\text{mA}$		10	200	mV	
Reset Threshold Voltage	V_{RT}	$T_j = 25^\circ\text{C}$	B	4.60	4.8	4.95	V
			C	4.30	4.5	4.65	V
			D	4.00	4.2	4.35	V
			E	3.70	3.9	4.05	V
			F	3.40	3.6	3.75	V
			G	3.10	3.3	3.45	V
			H	2.80	3.0	3.15	V
						50	100
Reset Threshold Hysteresis Voltage	V_{RTH}						
Reset Output Delay Time	t_d	$c_d = 0.1\mu\text{F}$	7.5	10	12.5	msec	
Output Pin Leakage Current	I_{OLEAK}	$V_{IN} = 0$, $V_o = 6\text{V}$	0.001	2		μA	
Reset Output Pin Leakage Current	I_{ORLEAK}	$V_{IN} = 0$, $V_{OR} = 6\text{V}$	0.001	2		μA	

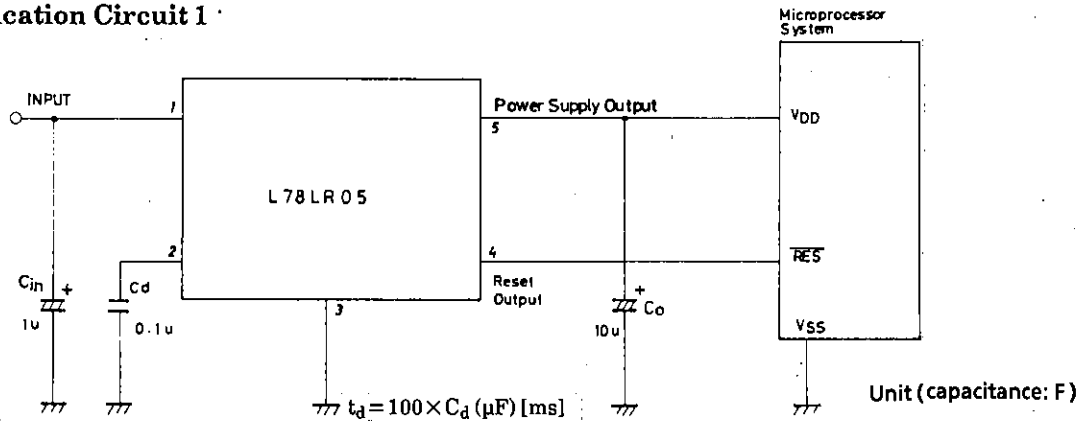
Equivalent Circuit Block Diagram



Unit (resistance: Ω , capacitance: F)

L78LR05

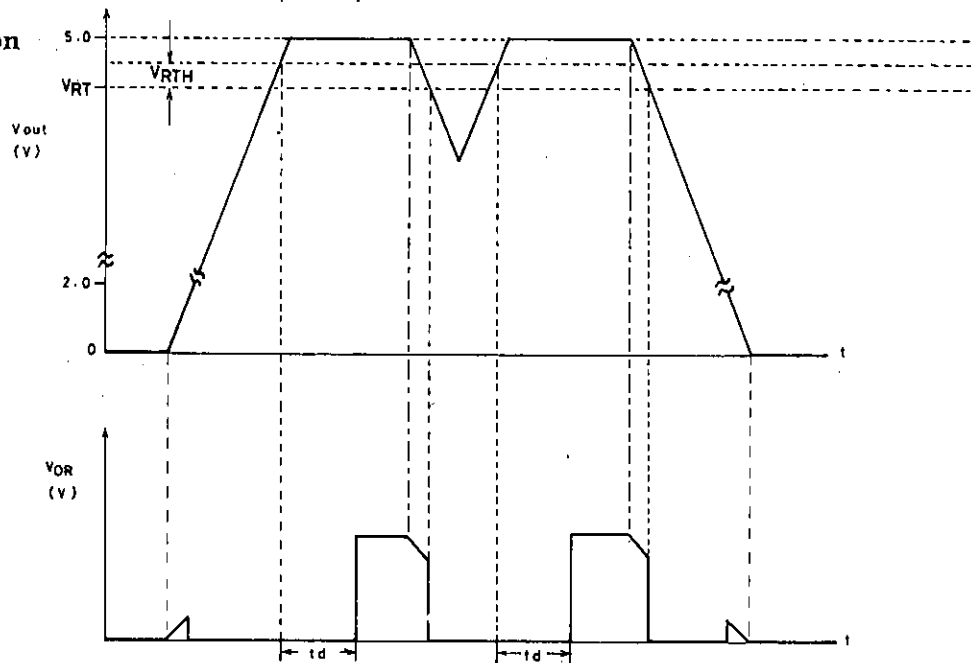
Sample Application Circuit 1



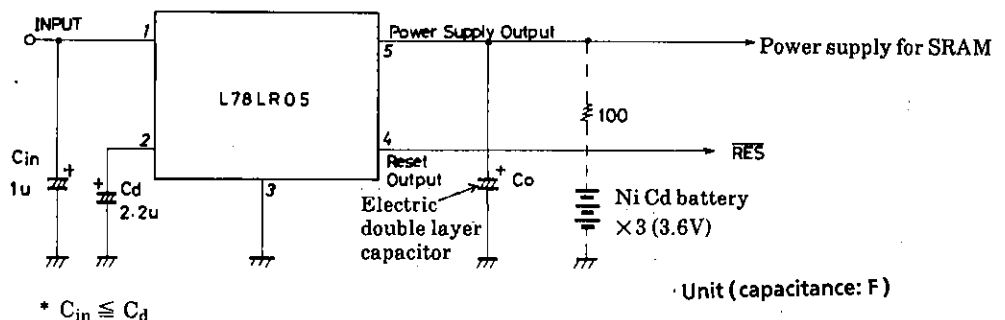
Note 1: When the capacitance of C_d is large, the capacitor may not discharge completely, causing t_d to be made shorter than a set value. If this is a problem, either connect a high speed diode (DS442) between pin2 (anode side) and pin5 (cathode side) or ensure an adequate discharge time by using values for capacitors C_{in} and C_d such that $C_{in} > C_d$.

Note 2: If a pull-up resistor is connected to the reset output pin externally, it is possible to cause a sink current up to 4mA to flow.

Reset Operation



Sample Application Circuit 2 (Direct battery backup)



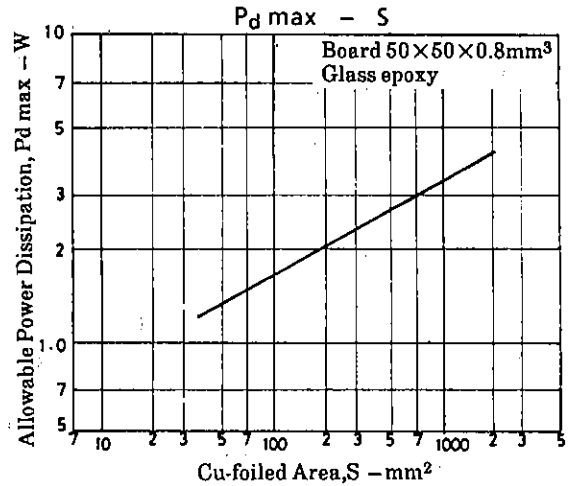
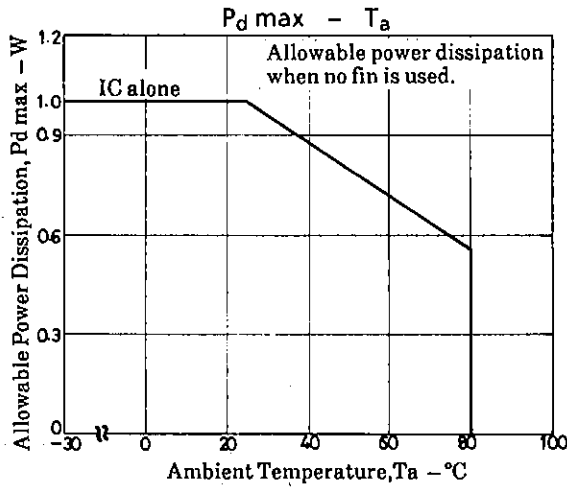
Since the leakage current at the output pin (pin5) of the L78LR05 is so low as 2µA or less, a backup circuit can be implemented by connecting an electric double layer capacitor (super capacitor: NEC, gold capacitor: Matsushita Electric) or a Ni Cd battery direct to the output pin. Since a reverse blocking diode, which has been so far connected to the output pin, is not required, a regulated power-supply voltage can be supplied to a load during the steady-state operation, without voltage drop caused by the diode and effects of temperature characteristics, current characteristics of the diode. No battery-regulator switching circuit is required at the battery backup start mode.

Note 3: The capacitance of reset output signal delay capacitor C_d must exceed that of input capacitor C_{in} . If the capacitance of C_d is small, a reset pulse signal may be generated once when the main power source is turned off (at the battery backup start mode).

L78LR05

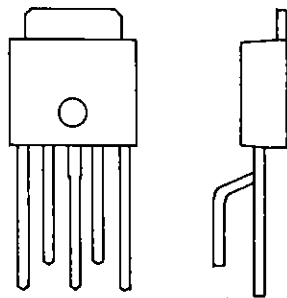
Allowable Power Dissipation

The allowable power dissipation is 1.0W ($T_a=25^\circ\text{C}$) with no fin attached. When the L78LR05 is surface-mounted on a hybrid IC board or printed circuit board, a high allowable power dissipation can be obtained, though it is placed in a small-sized package. Shown below is the relationship between the Cu-foiled area and the allowable power dissipation when the L78LR05 is surface-mounted on a glass epoxy board ($50\times 50\times 0.8\text{mm}^3$).

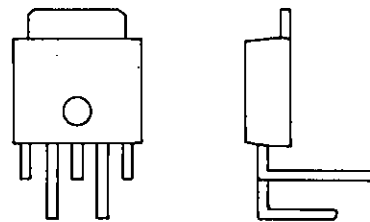


* The measured values of P_d represent the values measured when solder on the Cu-foiled area is all wet.

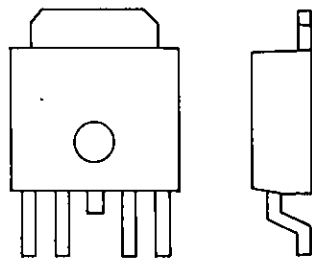
Lead Formings



MA forming

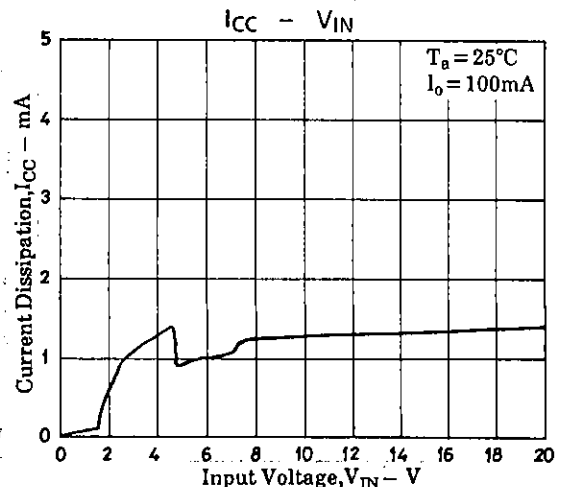
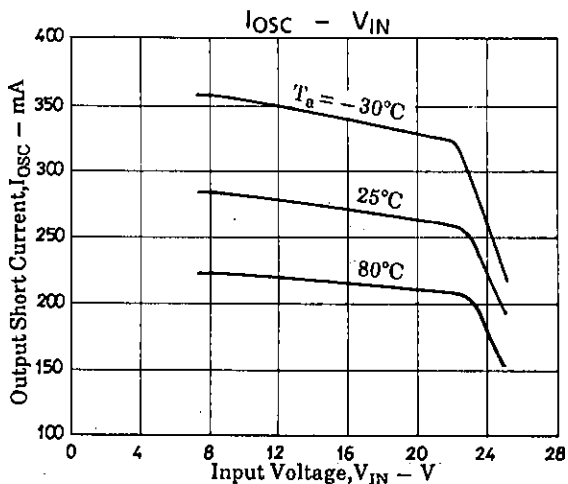
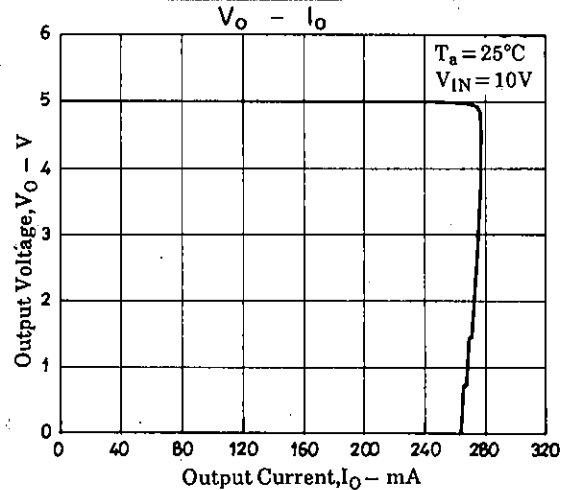
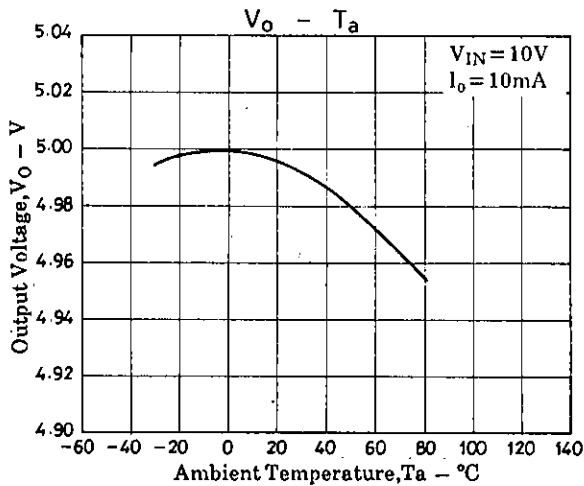
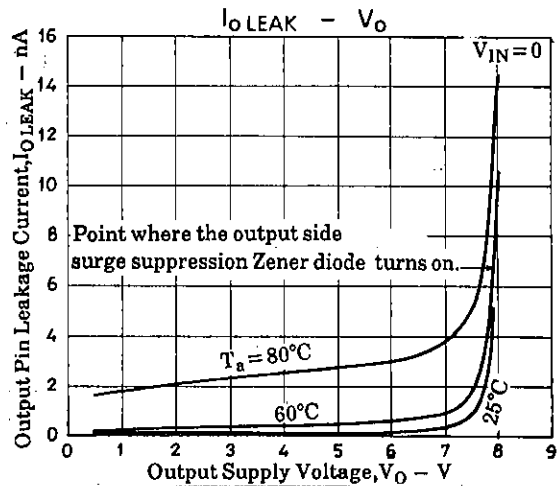
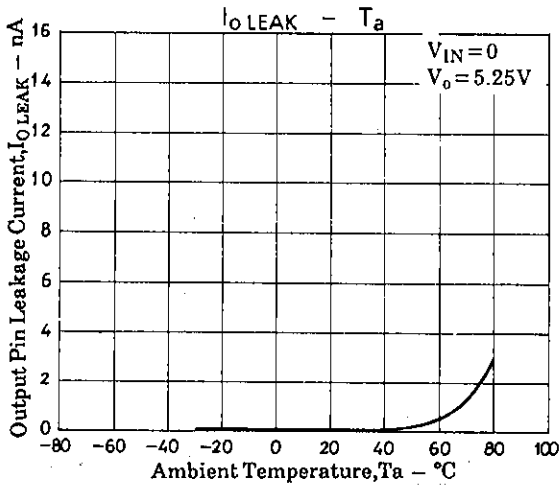
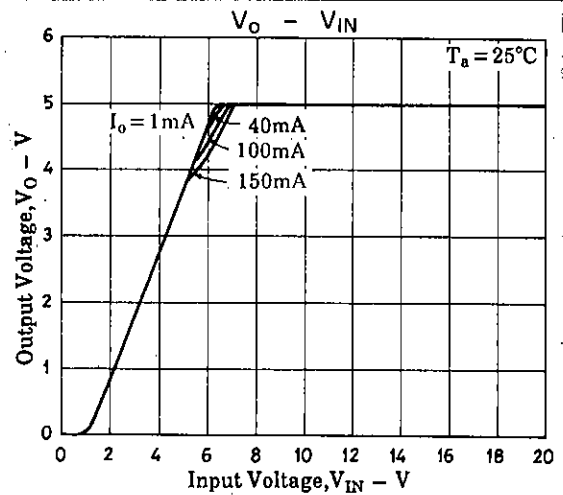
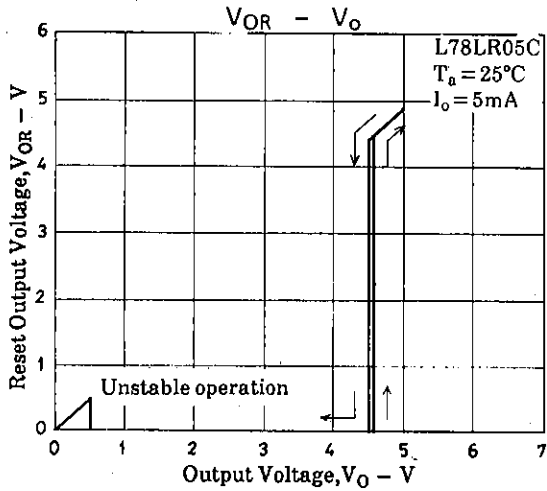


LR forming

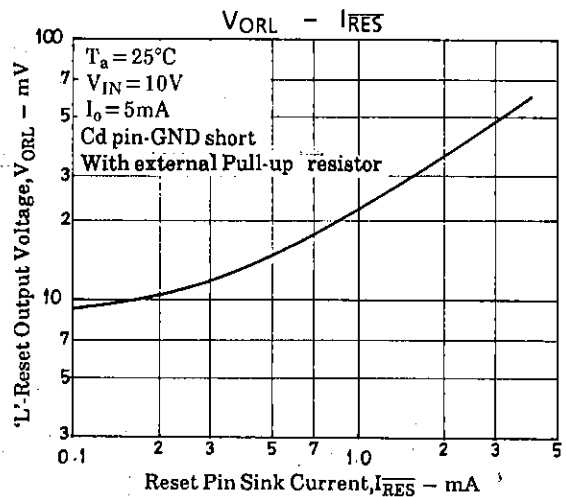
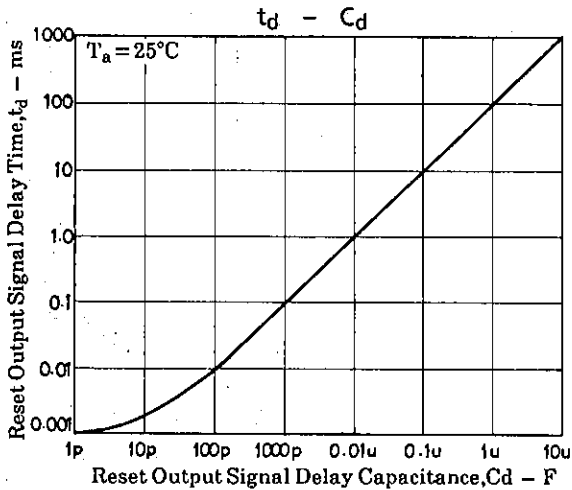
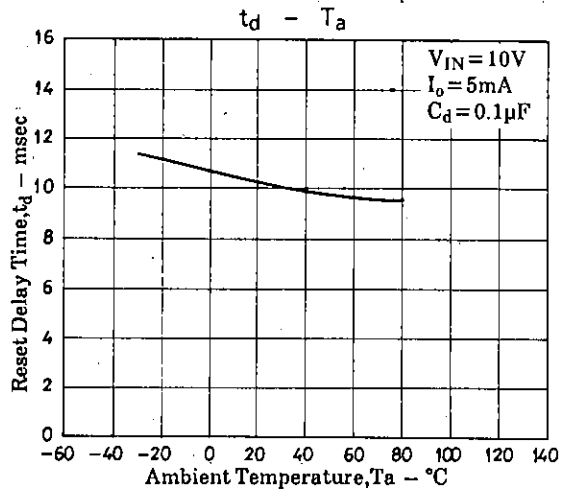
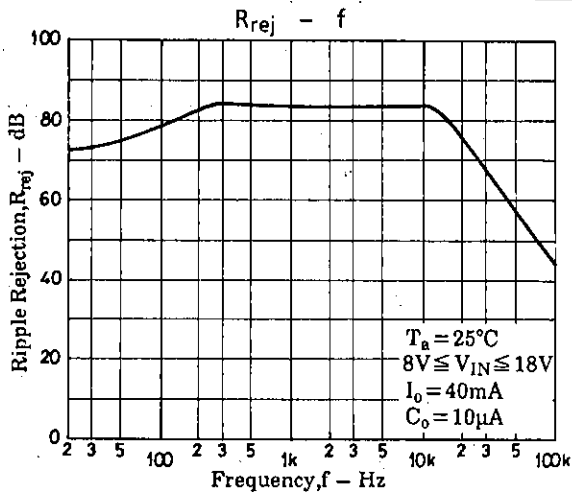


FA forming

L78LR05



L78LR05



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.