

TOSHIBA Diode Silicon Epitaxial Schottky Barrier Type

# DSF521

## High Speed Switching Application

Low forward voltage :  $V_F(3) = 0.5V$  (max.)

### Absolute Maximum Ratings (Ta = 25°C)

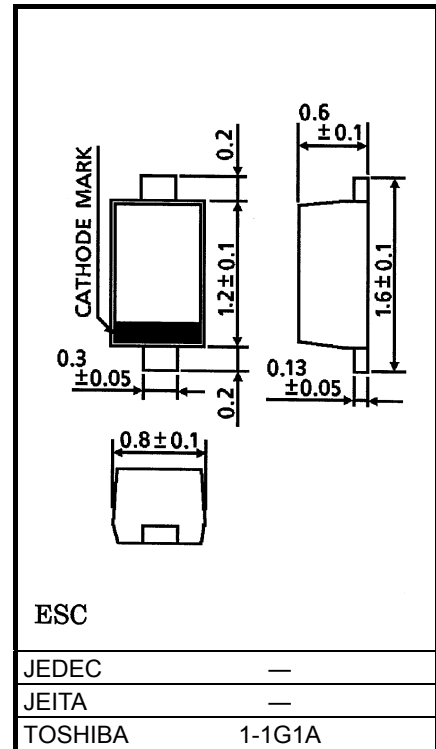
Characteristic	Symbol	Rating	Unit
Reverse voltage	$V_R$	30	V
Maximum (peak) forward current	$I_{FM}$	300	mA
Average forward current	$I_O$	200	mA
Surge current (10ms)	$I_{FSM}$	1	A
Power dissipation	$P^*$	150	mW
Junction temperature	$T_j$	125	°C
Storage temperature range	$T_{stg}$	-55 to 125	°C
Operating temperature range	$T_{opr}$	-40 to 100	°C

\*: Mounted on a glass epoxy circuit board of 20 × 20 mm, pad dimension of 4 × 4 mm.

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

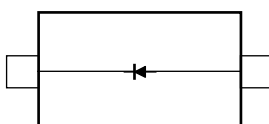


JEDEC —  
JEITA —  
TOSHIBA 1-1G1A  
Weight: 1.4 mg (typ.)

### Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 1$ mA	—	0.2	—	V
	$V_F(2)$	—	$I_F = 5$ mA	—	0.24	—	
	$V_F(3)$	—	$I_F = 200$ mA	—	0.45	0.5	
Reverse current	$I_R(1)$	—	$V_R = 10$ V	—	—	20	μA
	$I_R(2)$	—	$V_R = 30$ V	—	—	30	
Total capacitance	$C_T$	—	$V_R = 0, f = 1$ MHz	—	32	—	pF

### Equivalent Circuit (top view)



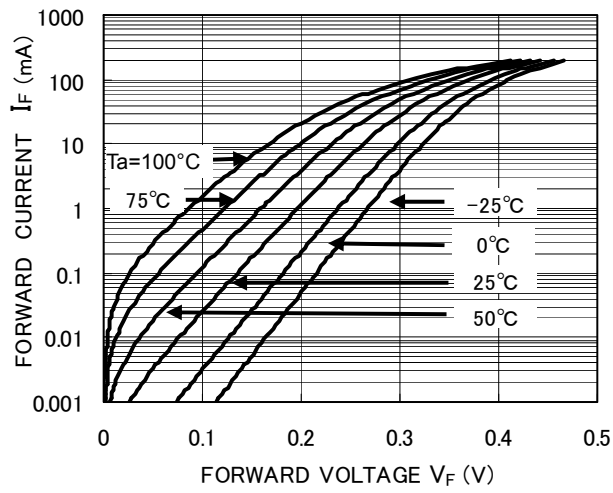
### Marking



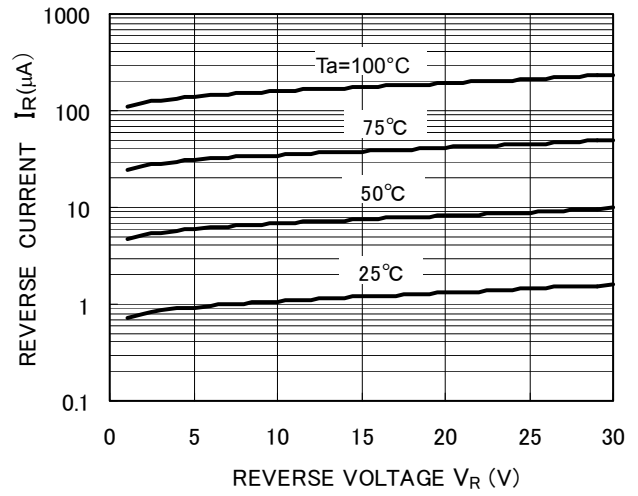
**Handling Precaution**

Schottky barrier diodes have reverse current characteristic compared to the other diodes.  
There is a possibility SBD may cause thermal runaway when it is used under high temperature or high voltage.  
Please take forward and reverse loss into consideration during design.

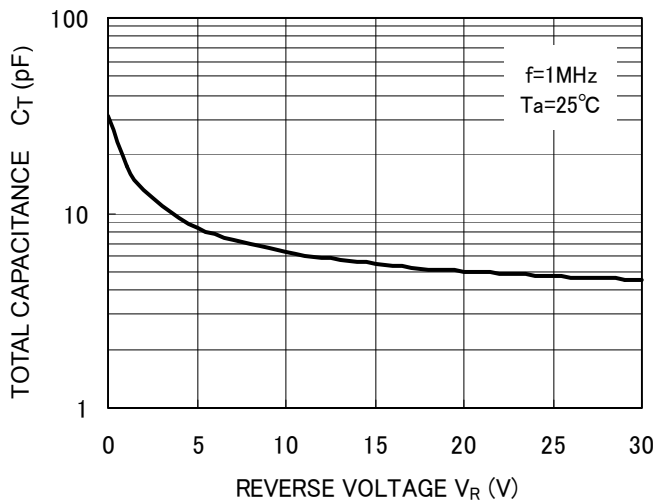
$I_F - V_F$



$I_R - V_R$



$C_T - V_R$



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