



LA5312V

Variable Divided Voltage Generator for LCDs

Overview

The LA5312V is a variable divided voltage generator IC for multiple drive of LCD matrix.

Features

- Power supply for variable bias LCD drive (1/5 to 1/19 bias available by internal resistors)
- Four voltage outputs generated by four operational amplifiers.
- Low current drain (0.18 mA typ.)
- Miniflat package for miniaturization.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{EE \text{ max}}$	$V_{CC} - V_{EE}$	36	V
Maximum output current	$I_{OUT \text{ max}}$	V1 - V4	*Internal	mA
Allowable power dissipation	$P_d \text{ max}$		330	mW
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

Note 1: Continuous operation (without damage) is guaranteed in the above ranges.

Note 2: *The maximum output current is the value stipulated under the test conditions on page 4.

Note 3: Output pins V1 to V4-to- V_{CC} or GND short not exceeding 1 ms is acceptable. ($|V_{CC} - V_{EE}| < 35 \text{ V}$)

Operating Conditions at $T_a = 25^\circ\text{C}$

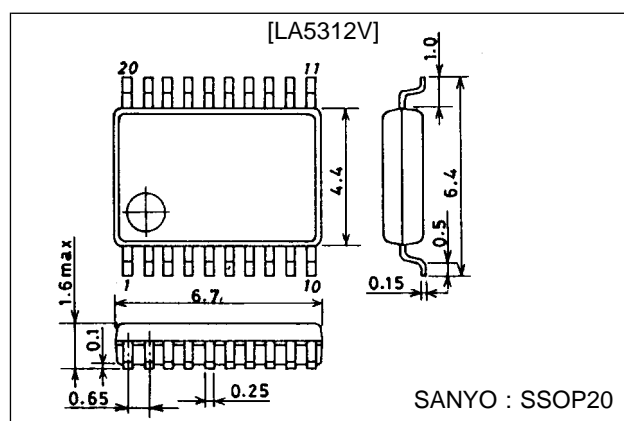
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	$V_{CC} - V_{EE}$	-35.5 to -6	V
Input voltage	V_{REF}	$V_{REF} \cong V_{EE} : V_{CC} - V_{REF}$	-35 to -6	V
Output current	$I_{OUT1,2}$	V1, V2	-0.5 to +5	mA
	$I_{OUT3,4}$	V3, V4	-10 to +5	mA

Note 4: Set V_{CC} and V_{EE} so that $|V1|$ and $|V_{EE} - V4|$ are 1 V or more.

Package Dimensions

unit : mm

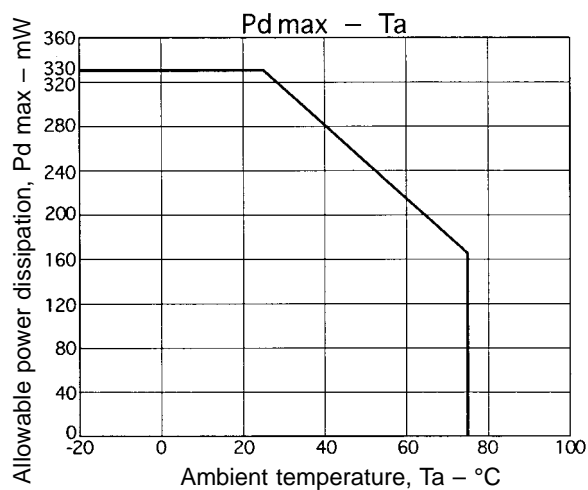
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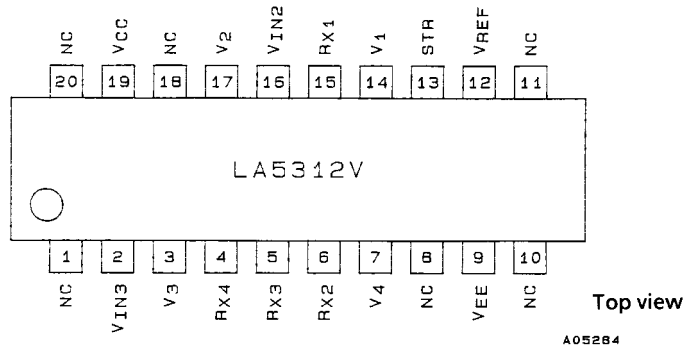
Operating Characteristics at Ta = 25°C, V_{CC} - V_{EE} = 20 V, V_{REF} = V_{EE}, R_X = 8 R

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I _{CC} , I _{EE}	STR = 5 V : V _{CC} , V _{EE}		0.18	0.3	mA
Input current	I _{STR}	STR = 5 V : STR		9	12	μA
Output voltage ratio	Ra1	V2 / V1	1.96	2.00	2.04	—
	Ra2	(V _{REF} - V3) / (V _{REF} - V4)	1.96	2.00	2.04	—
	Rb1	V _{REF} / V1	11.64	12.00	12.36	—
	Rb2	V _{REF} / V2	5.82	6.00	6.18	—
	Rb3	V _{REF} / (V _{REF} - V3)	5.82	6.00	6.18	—
Internal resistance ratio	R _{X1}	Referenced to R across : R _{X1} - R _{X2} : R _{X1} - R _{X3}		8		—
	R _{X2}			12		—
	R _{X3}	R _{X4} and V _{IN3} : R _{X1} - R _{X4} : R _{X1} - V _{IN3}		14		—
	R _{X4}			15		—
Resistance value	R	R value when voltage is applied across R _{X4} and V _{IN3} is 0.5 V : R _{X4} - V _{IN3}		30		kΩ
Load regulation	ΔV1	+0.1 mA < I _{OUT1} < +5 mA : V1			±20	mV
	ΔV2	+0.1 mA < I _{OUT2} < +5 mA : V2			±20	mV
	ΔV3	+0.1 mA < I _{OUT3} < +5 mA : V3			±20	mV
	ΔV4	+0.1 mA < I _{OUT4} < +5 mA : V4			±20	mV
	-ΔV1	-0.5 mA < I _{OUT1} < -0.1 mA : V1			±20	mV
	-ΔV2	-0.5 mA < I _{OUT2} < -0.1 mA : V2			±20	mV
	-ΔV3	-10 mA < I _{OUT3} < -0.1 mA : V3			±20	mV
-ΔV4	-10 mA < I _{OUT4} < -0.1 mA : V4 (Source I _{OUT} is negative and sink I _{OUT} is positive).			±20	mV	

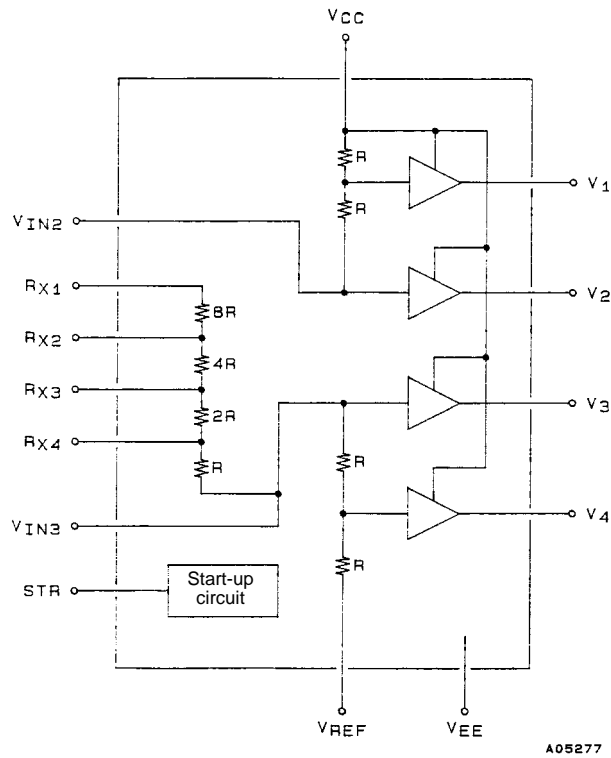


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Pin Assignment

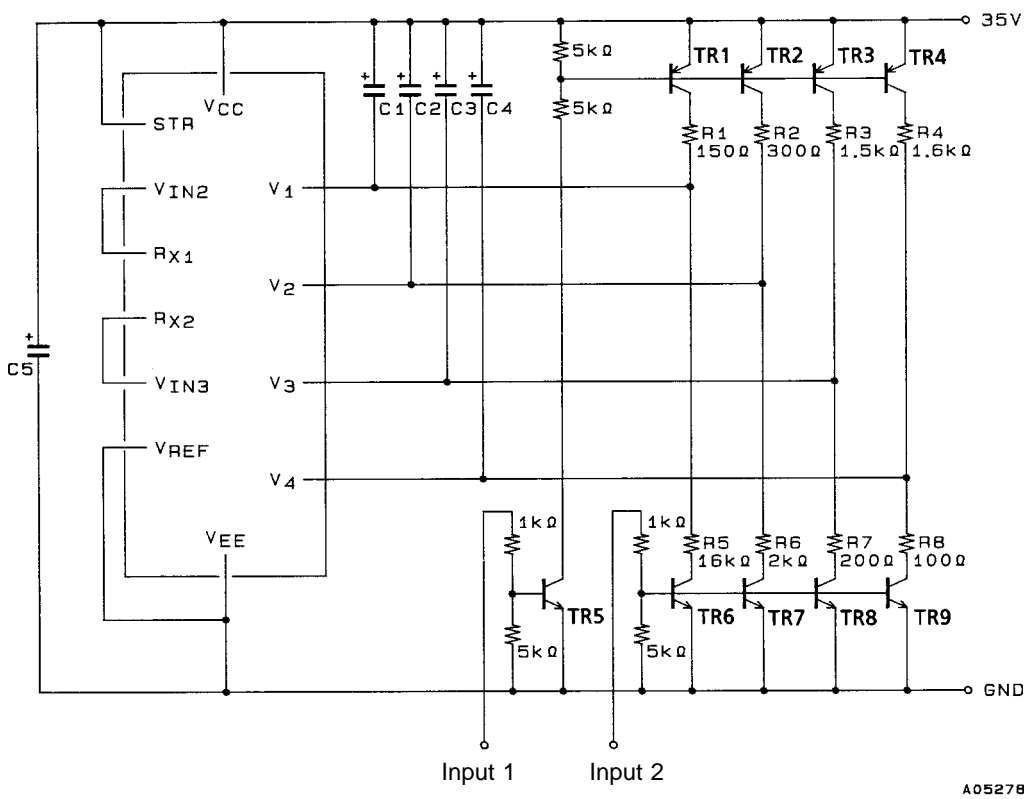


Block Diagram



(The voltages V_{RX1} , V_{RX2} , V_{RX3} , and V_{RX4} must obey the relationship $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4}$).

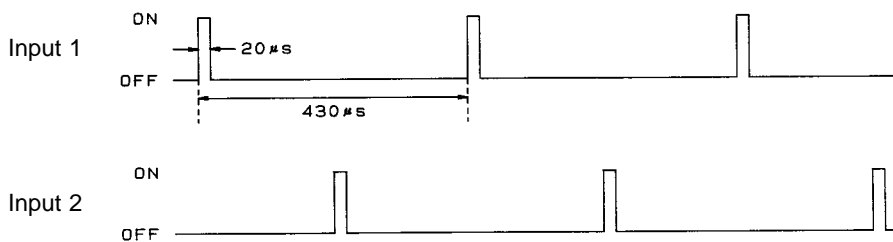
Maximum Output Current Load Test Conditions



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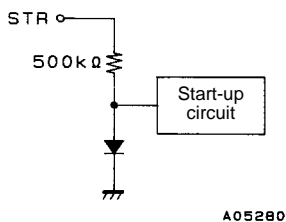
$V_{CC} - V_{EE} = 35\text{ V}$ $R_X = 8\text{ R}$ $C1\text{ to }4 = 10\ \mu\text{F}$ $C5 = 33\ \mu\text{F}$ $\text{R: } 1\text{ W or more}$
 TR1 to 4: 2SA984 E or F rank
 TR5 to 9: 2SC2274 E or F rank

The output load resistor values (R1 to R8) are set so that when an “on” level signal is input to inputs 1 and 2, a current of 15 to 30 mA max. flows to the sink side and the source side (approximately 2 mA on the V1 source side).



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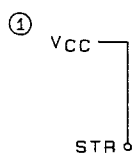
STR Pin Usage



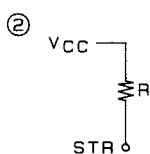
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The STR input is configured as shown left.

- The STR is either shorted with V_{CC} or connected to V_{CC} via an external resistor.
- It is possible to use a separate power supply (V_{IN}) such that $2\text{ V} < V_{IN} < V_{CC}$ for current saving.

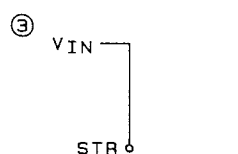


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(2 V or more required for STR)

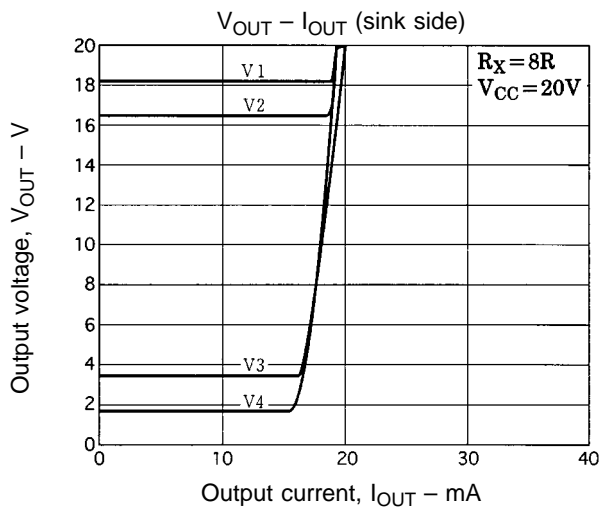
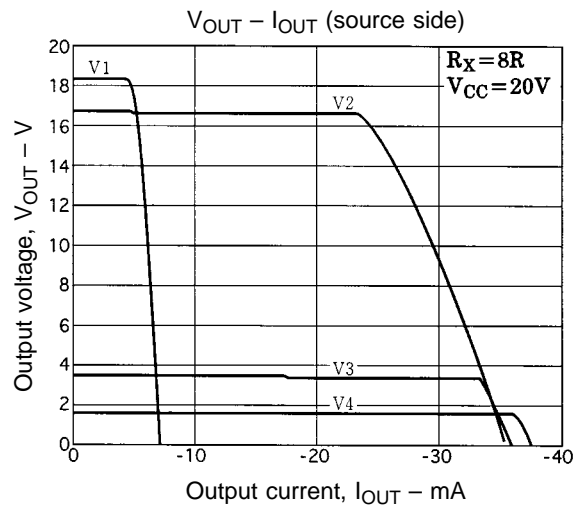
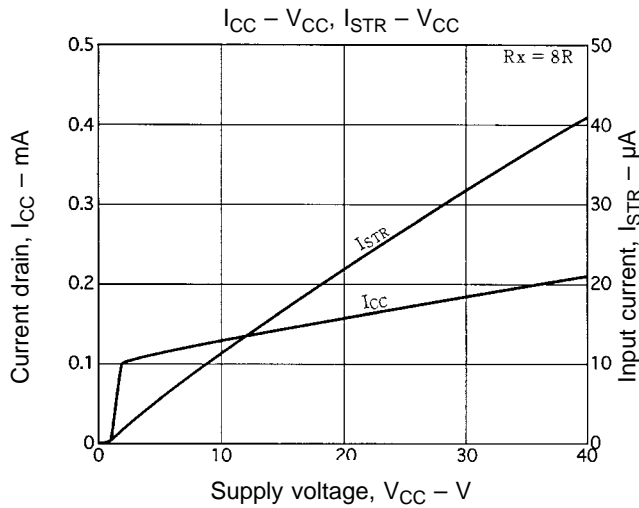
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($2\text{ V} < V_{IN} < V_{CC}$)

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