

# HVL388C

## Variable Capacitance Diode for VCO

REJ03G0363-0200  
Rev.2.00  
Mar 15, 2006

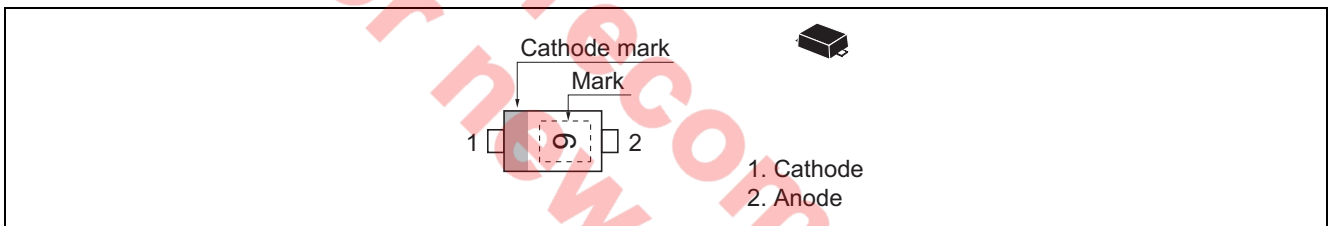
### Features

- High capacitance ratio. ( $n = 1.880$  min)
- Low series resistance. ( $r_s = 0.75 \Omega$  max)
- Extremely small Flat Lead Package (EFP) is suitable for surface mount design.

### Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVL388C	9	EFP	PXSF0002ZA-A

### Pin Arrangement



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	$V_R$	15	V
Junction temperature	$T_j$	125	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

## Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	$I_{R1}$	—	—	10	nA	$V_R = 15\text{ V}$
	$I_{R2}$	—	—	50		$V_R = 15\text{ V}, T_a = 60^\circ\text{C}$
Capacitance	$C_1$	3.162	—	3.465	pF	$V_R = 1\text{ V}, f = 1\text{ MHz}$
	$C_3$	1.570	—	1.720		$V_R = 3\text{ V}, f = 1\text{ MHz}$
Capacitance ratio	n	1.880	—	2.150	—	$C_1 / C_3$
Series resistance	$r_s$	—	—	0.75	$\Omega$	$V_R = 1\text{ V}, f = 470\text{ MHz}$

Note: For EFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

### Main Characteristic

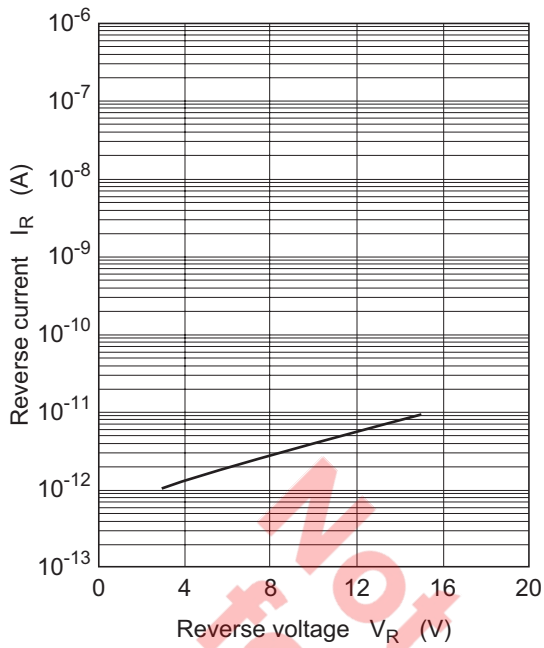


Fig.1 Reverse current vs. Reverse voltage

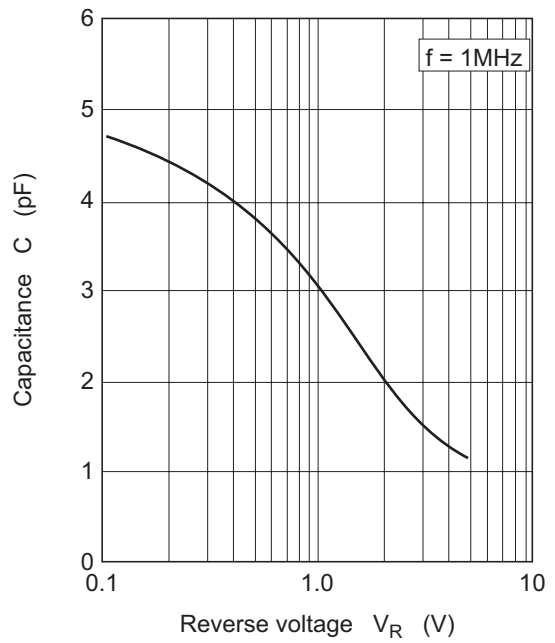


Fig.2 Capacitance vs. Reverse voltage

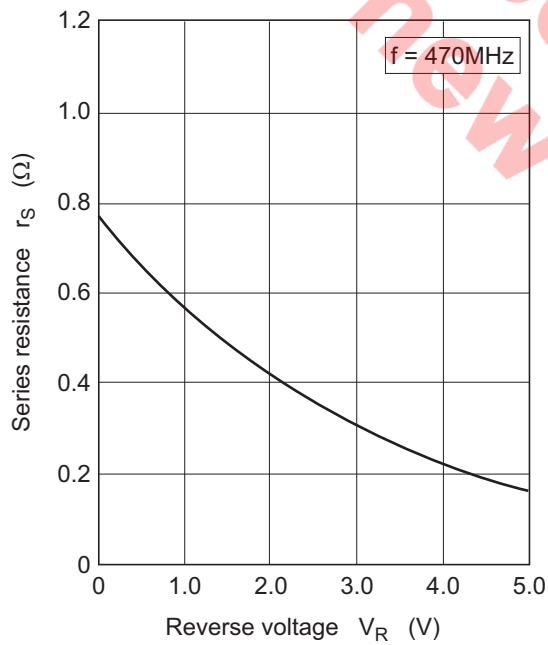
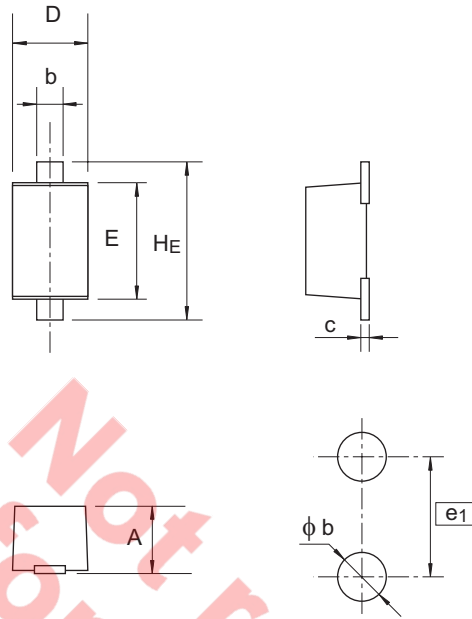


Fig.3 Series resistance vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
EFP	—	PXSF0002ZA-A	EFP / EFPV	0.0007g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.44	0.47	0.50
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.75	0.80	0.85
$H_E$	0.95	1.00	1.05
$\phi b$	—	0.40	—
$e_1$	—	1.00	—

Not recommended for new design

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