

# MTM78E2B0LBF

## Silicon N-channel MOS FET

For lithium-ion secondary battery protection circuit

### ■ Overview

MTM78E2B0LBF is the low ON resistance dual N-channel MOS FET designed for lithium-ion secondary battery protection circuit.

### ■ Features

- Low drain-source ON resistance:  $R_{DS(on)}$  typ. = 21.5 m $\Omega$  ( $V_{GS} = 4$  V)
- Small size surface mounting package: WSMINI8-F1-B (2.1 mm  $\times$  2.0 mm  $\times$  0.7 mm)
- Drain common 2 elements
- 2.5V drive
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

### ■ Packaging

MTM78E2B0LBF Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	$V_{DSS}$	20	V
Gate-source surrender voltage	$V_{GSS}$	$\pm 12$	V
Drain current	$I_D$	4.0	A
Peak drain current *1	$I_{DP}$	40	A
Power dissipation	$P_{D1}$ *2	700	mW
	$P_{D2}$ *3	150	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Note) \*1:  $t = 10$  s, Duty cycle  $< 1\%$

\*2: Ceramic substrate (70 mm  $\times$  70 mm  $\times$  1.0 mm), dual operating.

\*3: Stand-alone (without the board)

### ■ Package

#### • Code

WSMini8-F1-B

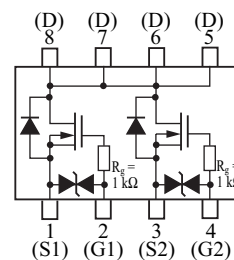
Package dimension clicks here.→

#### • Pin Name

- |             |          |
|-------------|----------|
| 1: Source-1 | 5: Drain |
| 2: Gate-1   | 6: Drain |
| 3: Source-2 | 7: Drain |
| 4: Gate-2   | 8: Drain |

### ■ Marking Symbol: 5A

### ■ Internal Connection



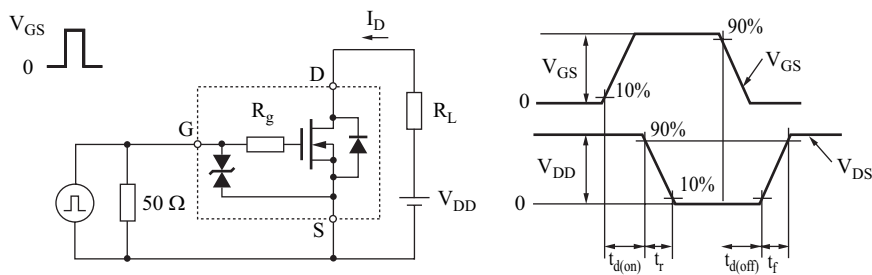
### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

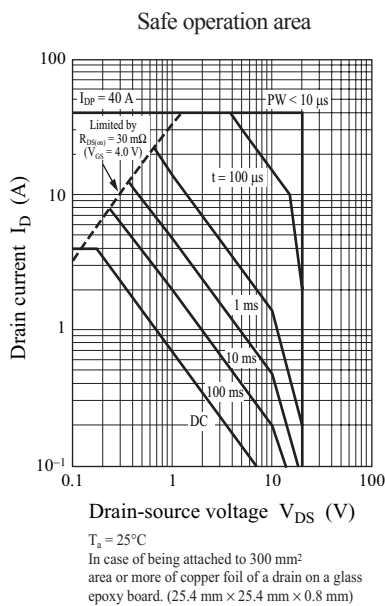
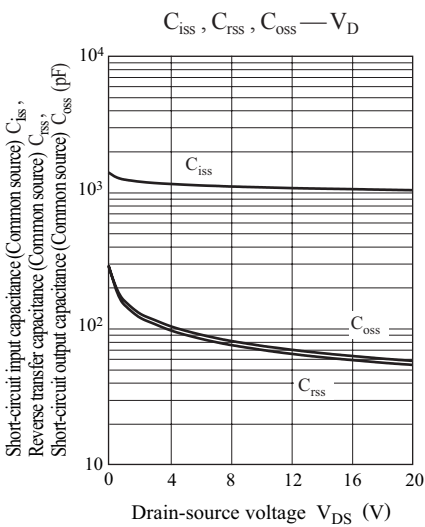
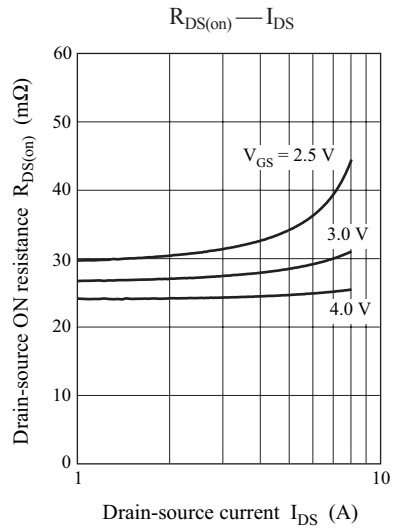
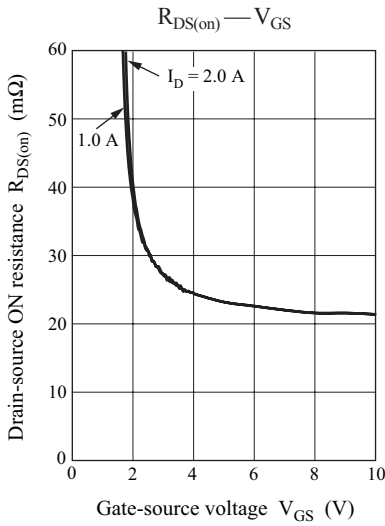
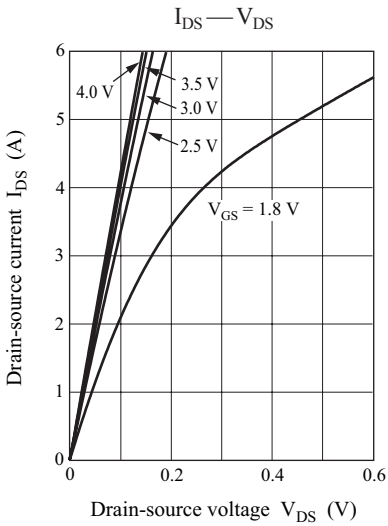
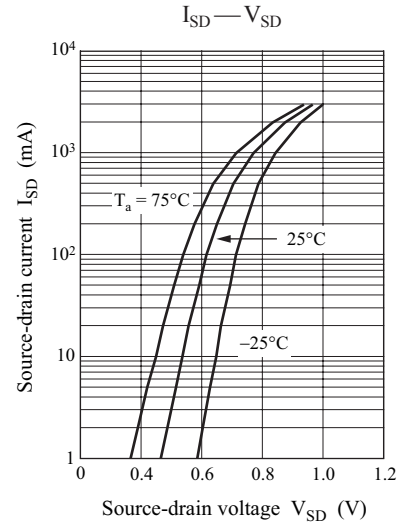
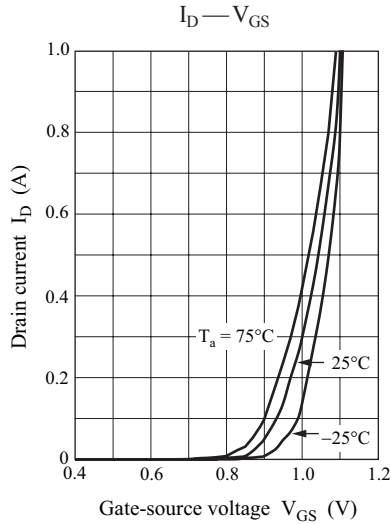
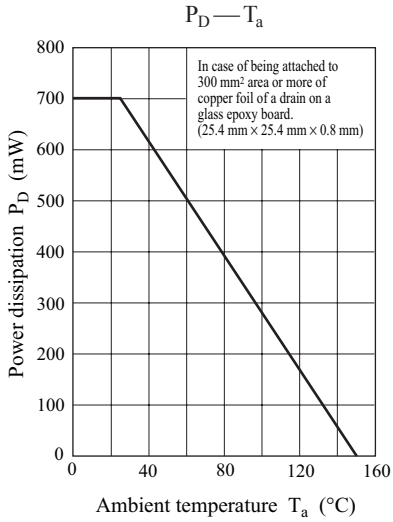
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	$V_{DSS}$	$I_D = 1.0 \text{ mA}, V_{GS} = 0$	20			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$			$\pm 10$	$\mu\text{A}$
Gate threshold voltage	$V_{TH}$	$I_D = 1.0 \text{ mA}, V_{DS} = 10 \text{ V}$	0.40	0.85	1.3	V
Drain-source ON resistance 1	$R_{DS(on)1}$	$I_D = 2.0 \text{ A}, V_{GS} = 4.0 \text{ V}$		21.5	25.0	$\text{m}\Omega$
Drain-source ON resistance 2	$R_{DS(on)2}$	$I_D = 1.5 \text{ A}, V_{GS} = 3.0 \text{ V}$		26.0	30.0	$\text{m}\Omega$
Drain-source ON resistance 3	$R_{DS(on)3}$	$I_D = 1.0 \text{ A}, V_{GS} = 2.5 \text{ V}$		30.0	36.0	$\text{m}\Omega$
Forward transfer admittance	$ Y_{fs} $	$I_D = 1.0 \text{ A}, V_{DS} = 10 \text{ V}$	1.0			S
Short-circuit input capacitance (Common source)	$C_{iss}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		1 100		pF
Short-circuit output capacitance (Common source)	$C_{oss}$			75		pF
Reverse transfer capacitance (Common source)	$C_{rss}$			70		pF
Turn-on delay time *	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, V_{GS} = 4.0 \text{ V},$ $I_D = 1.0 \text{ A}, R_L = 10 \Omega$		0.20		$\mu\text{s}$
Rise time *	$t_r$			0.50		$\mu\text{s}$
Turn-off delay time *	$t_{d(off)}$			2.0		$\mu\text{s}$
Fall time *	$t_f$			1.5		$\mu\text{s}$

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*1:  $t = 10 \mu\text{s}$ , Duty cycle  $< 1\%$

\*2: Measurement circuit





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