Slew Rate Controlled Load Switch

FEATURES

- **1.8 V to 5.5 V Input Voltage range**
- **Very Low $R_{DS(ON)}$, typically 80 m (5 V)**
- Slew rate limited turn–on time options
- SiP4280–1: 1 ms
- SiP4280–3: 100 μs
- Fast shutdown load discharge option
- Low quiescent current
- 4 kV ESD Rating
- 8 pin SC70JW package

APPLICATIONS

- Cellular telephones
- Digital still cameras
- Personal digital assistants (PDA)
- Hot swap supplies
- Notebook computers
- Personal communication devices

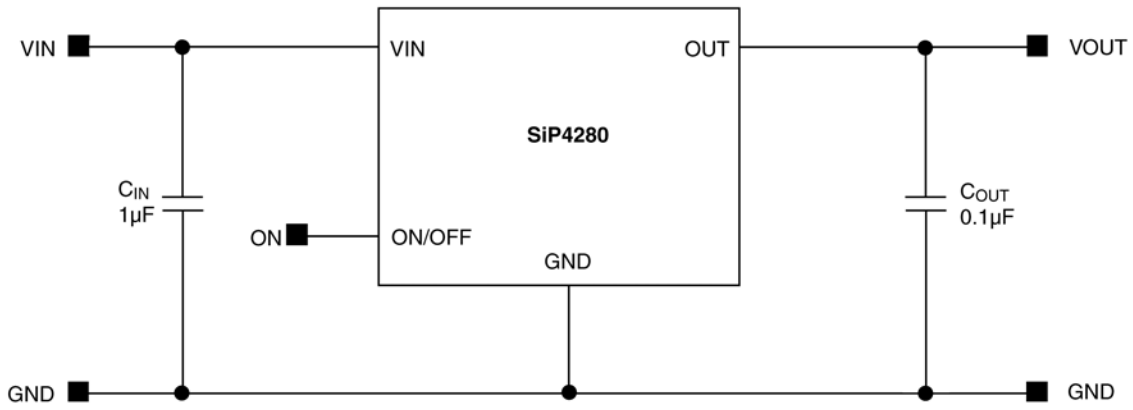
DESCRIPTION

The SiP4280 is a P–channel MOSFET power switch designed for high–side load switching applications. The output pass transistor is a P–channel MOSFET transistor with typically 80 mΩ $R_{DS(ON)}$. The SiP4280 is available in two different versions of turn–on times. The SiP4280–1 version has a slew rate limited turn–on time typically of 1 ms. The SiP4280–3 version has a slew rate limited turn–on time typically of 100 μs and additionally offers a shutdown load discharge circuit to rapidly turn off a load circuit when the switch is disabled.

Both SiP4280 load switch versions operate with an input voltage ranging from 1.8 V to 5.5 V, making them ideal for both 3 V and 5 V applications. The SiP4280 also features an under–voltage lock out which turns the switch off when an input undervoltage condition exists. Input logic levels are TTL and 2.5 volt to 5.0 volt CMOS compatible. The quiescent supply current is very low, typically 2.5 μA. In shutdown mode, the supply current decreases to less than 1.0 μA.

The SiP4280 is available in a 8 pin SC70JW package and is specified over –40 °C to 85 °C temperature range.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{IN}) . . . . . –0.3 V to 6 V
Enable Input Voltage (V_{ON}) . . . . . –0.3 V to 6 V
Output Voltage (V_{OUT}) . . . . . –0.3 V to V_{IN} +0.3 V
Maximum Switch Current (I_{MAX}) . . . . . 2.3 A
Maximum Pulsed Current (I_{DM}) . . . . . $V_{IN} \geq$ 2.5 V ..... 6 A
. . . . . V_{IN} < 2.5 V ..... 3 A

Junction Temperature (T_J) . . . . . –40 °C to 150 °C
Thermal Resistance (θ_{JA})[a] . . . . . 140 °C/W
Power Dissipation (P_D)[b] . . . . . 714 mW

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.14 mW/°C above T_A = 25 °C

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{IN} . . . . . 1.8 V to 5.5 V
Operating Temperature Range . . . . . –40 °C to 85 °C

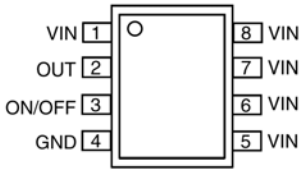
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 5 V, T_A = –40 °C to 85 °C	Limits Min[a]	Typ[b]	Max[a]	Units
SiP4280 All Versions						
Operating Voltage[c]	V_{IN}		1.8	–	5.5	V
Undervoltage Lockout	V_{UVLO}	V_{IN} Falling	1.0	1.4	1.8	V
Undervoltage Lockout Hysteresis	$V_{UVLO(hyh)}$		–	250	–	mV
Quiescent Current	I_Q	ON/OFF = active	–	2.5	4	µA
Off Supply Current	$I_{Q(OFF)}$	ON/OFF = inactive, OUT = open	–	0.01	1	µA
Off Switch Current	$I_{SD(OFF)}$	ON/OFF = inactive, V_{OUT} = 0	–	0.01	1	µA
On–Resistance	$R_{DS(on)}$	V_{IN} = 5 V, T_A = 25 °C	–	80	120	mΩ
		V_{IN} = 4.2 V, T_A = 25 °C	–	85	130	mΩ
		V_{IN} = 3 V, T_A = 25 °C	–	100	150	mΩ
		V_{IN} = 1.8 V, T_A = 25 °C	–	160	250	mΩ
On–Resistance Temp–Coefficient	TC_{RDS}		–	2800	–	ppm/°C
ON/OFF Input Low Voltage[d]	V_{IL}	V_{IN} = 2.7 V to 5.5 V	–	–	0.8	V
ON/OFF Input High Voltage	V_{IH}	V_{IN} = 2.7 V to ≤ 4.2 V	2	–	–	V
		V_{IN} = > 4.2 V to 5.5 V	2.4	–	–	V
ON/OFF Input Leakage	I_{SINK}	$V_{ON/OFF}$ = 5.5 V	–	–	1	µA
SiP4280–1 Version						
Output Turn–On Delay Time	$T_{D(ON)}$	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	20	40	µs
Output Turn–On Rise Time	T_{ON}	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	1000	1500	µs
Output Turn–Off Delay Time	$T_{D(OFF)}$	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	4	10	µs
SiP4280–3 Version						
Output Turn–On Delay Time	$T_{D(ON)}$	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	20	40	µs
Output Turn–On Rise Time	T_{ON}	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	100	150	µs
Output Turn–Off Delay Time	$T_{D(OFF)}$	V_{IN} = 5 V, R_{LOAD} = 10Ω, T_A = 25 °C	–	4	10	µs
Output Pull–Down Resistance	R_{PD}	ON/OFF = inactive, T_A = 25 °C	–	150	250	Ω

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Part requires minimum start–up of $V_{IN} \geq$ 2.0 to ensure operation down to 1.8 V.
d. For $V_{IN} \leq$ 2.7 V see typical ON/OFF threshold curve.

PIN CONFIGURATION

SC70JW-8 Package (Top View)



PIN DESCRIPTION

Pin Number SC70JW–8	Pin Name	Description
1,5,6,7,8	V_{IN}	This pin is the P–channel MODFET source connection
3	ON/OFF	Logic high enables the IC; logic low disables the IC and reduces the quiescent current to 2.5 μA
4	GND	Ground connection
2	OUT	This pin is the P–channel MOSFET drain connection.

SELECTION GUIDE

Part Number	Slew Rate (typ)	Active Pull Down	Enable
SiP4280–1–T1–E3	1 ms	No	Active High
SiP4280–3–T1–E3	100 μs	Yes	Active High

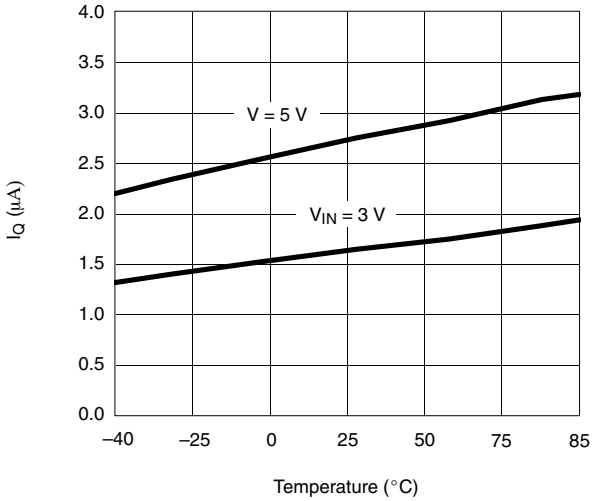
ORDERING INFORMATION

Part Number	Marking	Temperature Range	Package
SiP4280DR–1–T1–E3	L1XXX	–40 °C to 85 °C	SC70JW–8
SiP4280DR–3–T1–E3	L3XXX		SC70JW–8

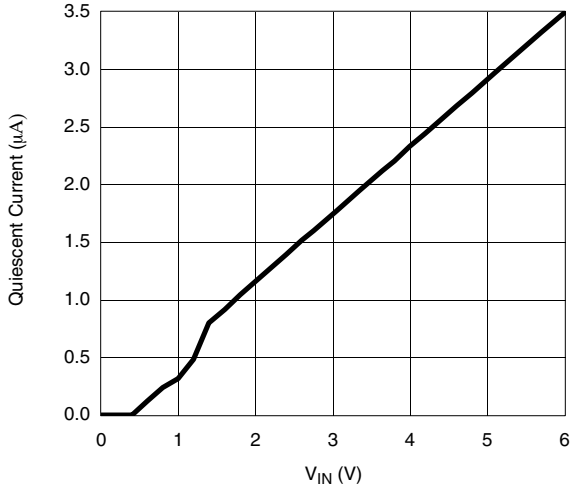
Notes:
XXX = Lot Code

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

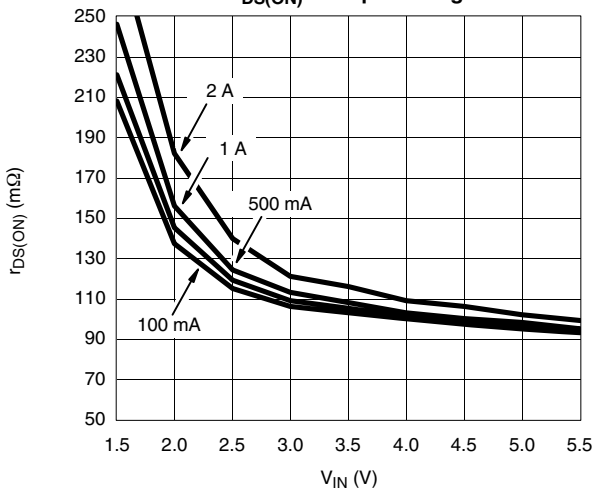
Quiescent Current vs. Temperature



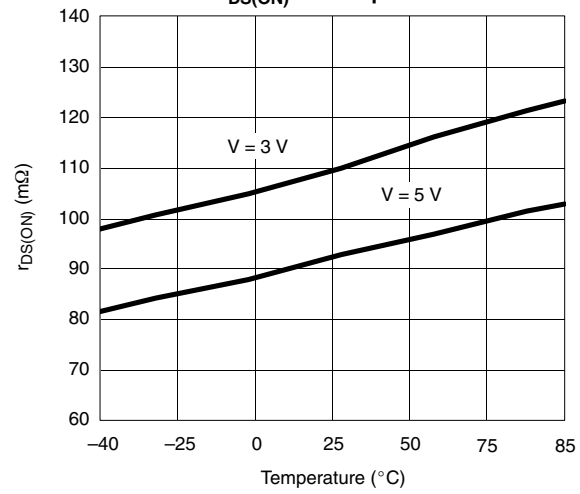
Quiescent Current vs. Input Voltage



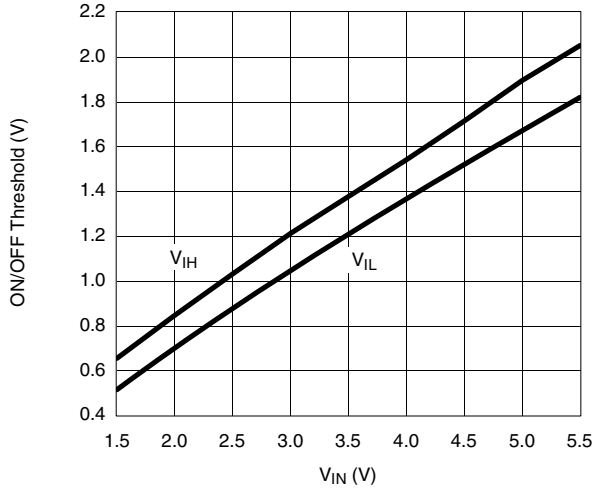
$R_{DS(ON)}$ vs. Input Voltage



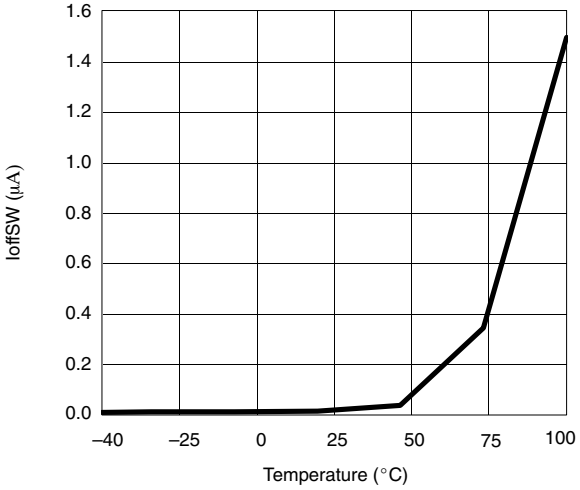
$R_{DS(ON)}$ vs. Temperature



ON/OFF Threshold vs. Input Voltage



Off Switch Current vs. Temperature



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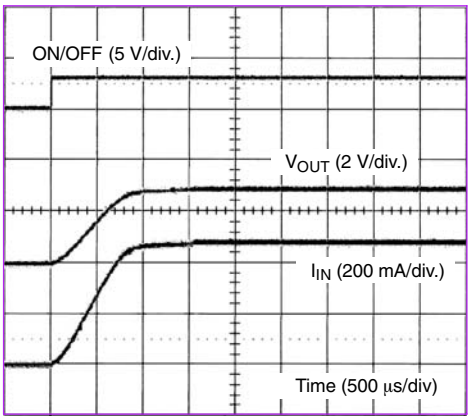
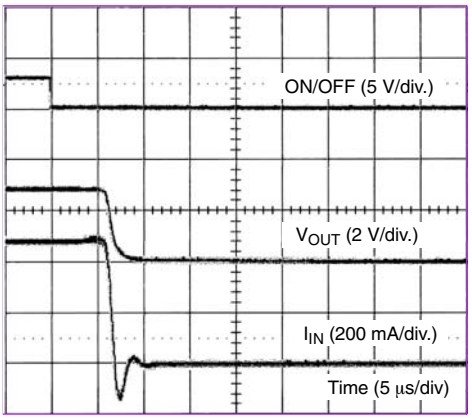
TYPICAL WAVEFORMS

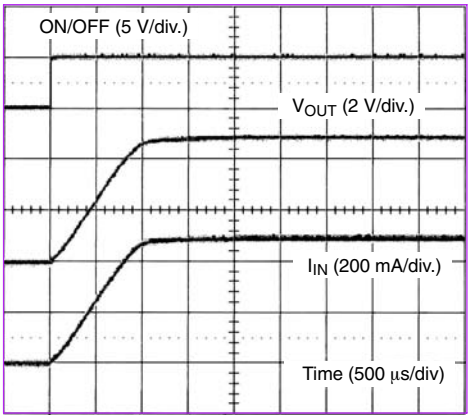
SiP4280–1 Turn–On (V_{IN} = 3 V, R_{LOAD} = 6 Ω)



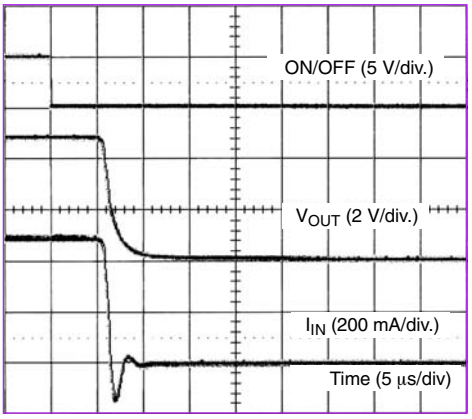
SiP4280–1 Turn–Off (V_{IN} = 3 V, R_{LOAD} = 6 Ω)



SiP4280–1 Turn–On (V_{IN} = 5 V, R_{LOAD} = 10 Ω)

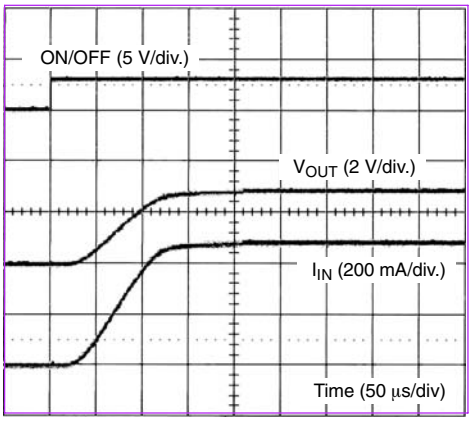


SiP4280–1 Turn–Off (V_{IN} = 5 V, R_{LOAD} = 10 Ω)

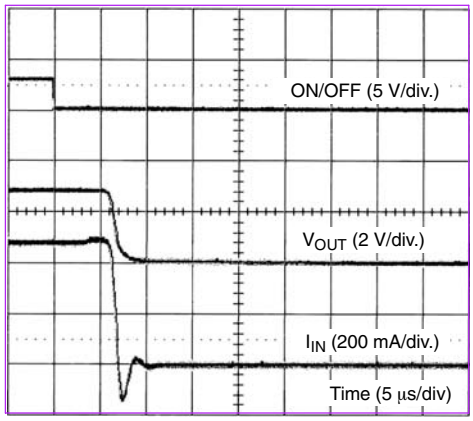


TYPICAL WAVEFORMS

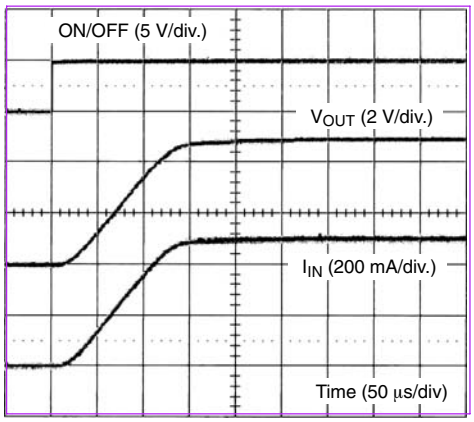
SiP4280–3 Turn–On (V_{IN} = 3 V, R_{LOAD} = 6 Ω)



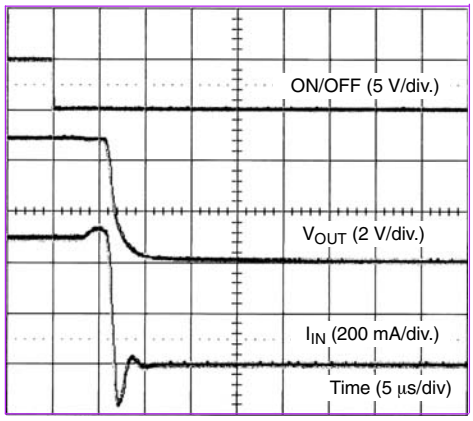
SiP4280–3 Turn–Off (V_{IN} = 3 V, R_{LOAD} = 6 Ω)



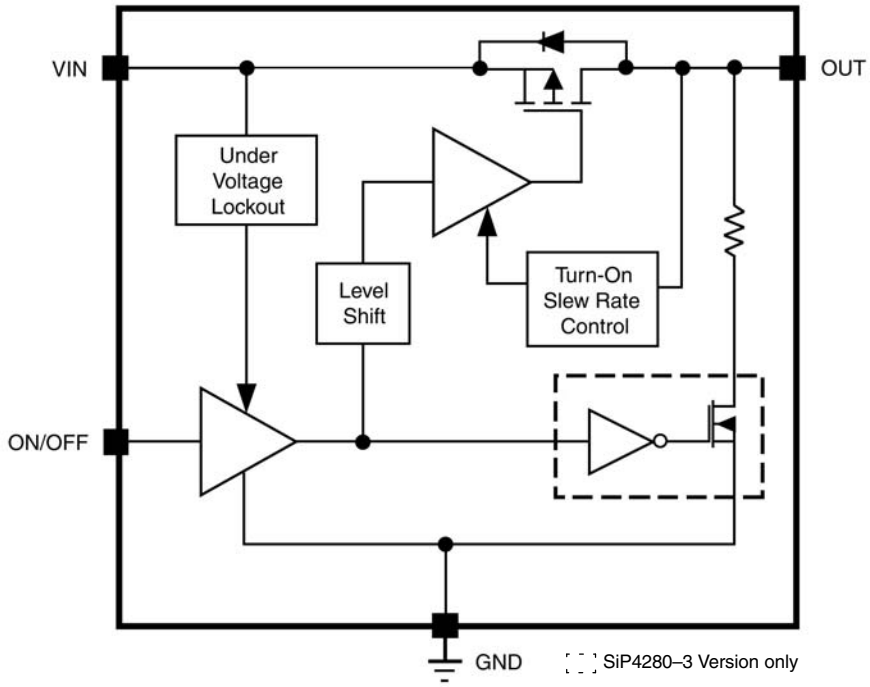
SiP4280–3 Turn–On (V_{IN} = 5 V, R_{LOAD} = 10 Ω)



SiP4280–3 Turn–Off (V_{IN} = 5 V, R_{LOAD} = 10 Ω)



BLOCK DIAGRAM



SiP4280 Functional Block Diagramm

DETAILED DESCRIPTION

The SiP4280 is a P–channel MOSFET power switches designed for high–side slew rate controlled load–switching applications. During turn on, the current ramps linearly until it reaches the level required for the output load condition. This is achieved by first applying the threshold voltage on the gate of the MOSFET. Once at this level, the current begins to slew and the gate voltage is then linearly increased until the MOSFET becomes fully enhanced. Once fully enhanced, the gate is quickly increased to the full input voltage and $R_{DS(ON)}$ is minimized.

The SiP4280–1 version has a moderate 1ms turn on slew rate feature, which reduces in–rush current when the MOSFET is turned on. This function allows the load switch to be implemented with a small input capacitor, or no input capacitor at all. The SIP4280–3 has in addition to the 100 μs minimized slew rate limited turn on function, a shutdown output discharge circuit to rapidly turn off a load when the load switch is disabled through the ON/OFF pin.

Both versions of the SiP4280 operate with input voltages ranging from 1.8 V to 5.5 V. Also, both versions of this device have extremely low operating current, making them ideal for battery–powered applications. In cases where the input voltage drops below 1.8 V, the under voltage lockout function will prevent the P–channel MOSFET device from entering into the saturation region of operation by automatically shutting down SiP4280. The ON/OFF control pin is TTL compatible and will also function with 2.5 volt to 5 volt CMOS logic systems.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 1 μF or larger capacitor for C_{IN} is recommended in almost all ap–plications. The Bypass capacitor should be placed as phy–sically close as possible to the SiP4280 to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 μF capacitor or larger across V_{OUT} and GND is recom–mended to insure proper slew operation. C_{OUT} may be increased without limit to accommodate any load transient condition with only minimal affect on the SiP4280 turn on slew rate time. There are no ESR or capacitor type requirement.

Enable

The ON/OFF pin is compatible with both TTL and CMOS logic voltage levels.

Reverse Voltage Conditions and Protection

The P–channel MOSFET pass transistor has an intrinsic diode that is reversed biased when the input voltage is greater than the output voltage. Should V_{OUT} exceed V_{IN} , this intrinsic diode will become forward biased and allow excessive current to flow into the IC thru the V_{OUT} pin and potentially damage the IC device. Therefore extreme care should be taken to prevent V_{OUT} from exceeding V_{IN}.

In conditions where V_{OUT} exceeds V_{IN} a Schottky diode in parallel with the internal intrinsic diode is recommended to protect the SiP4280.

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