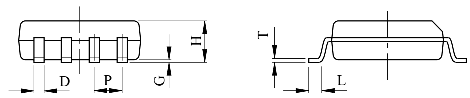
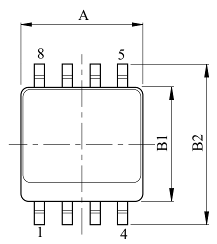
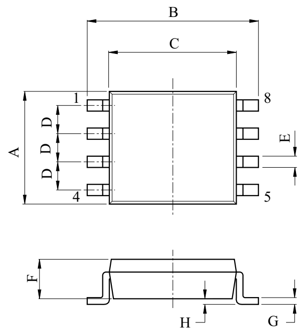
Gate Pulse Modulator.

- The KIA3820F/FK is specifically designed for application of TFT LCD glass panel.
- Flicker compensation circuit.
- Reduction of coupling effect between gate line and pixel.
- Power seguence circuit for gate dirvier IC.
- Operation from 15V to 38V positive supply input.
- Output delay time adjustable.

DIM	MILLIMETERS
A	4.85±0.2
B1	3.94±0.2
B2	6.02±0.3
D	0.4±0.1
G	0.15+0.1/-0.05
H	1.63±0.2
L	0.65±0.2
P	1.27
T	0.20+0.1/-0.05

FLP-8



DIM	MILLIMETERS
A	2.0±0.1
B	3.1±0.1
C	2.3±0.1
D	0.5
E	0.2+0.05/-0.04
F	0.7±0.1
G	0.12±0.04
H	0 ~ 0.1

US8

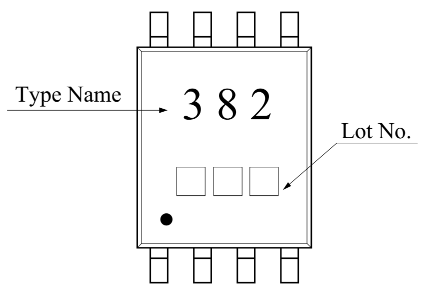
MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Positive Supply Voltage		V_{GH}	40	V
FLK Voltage		V_{FLK}	5	V
DPM Voltage		V_{DPM}	5	V
Output Current		I_O	30	mA
Power Dissipation	FK (US8)	P_D	200	mW
	F (FLP-8)		240	
Operating Temperature		T_{opr}	-20～85	℃
Storage Temperature		T_{stg}	-40～125	℃

LINE - UP

ITEM	FUNCTION	PACKAGE
KIA3820F	Gate Pulse Modulator	FLP-8
KIA3820FK		US8

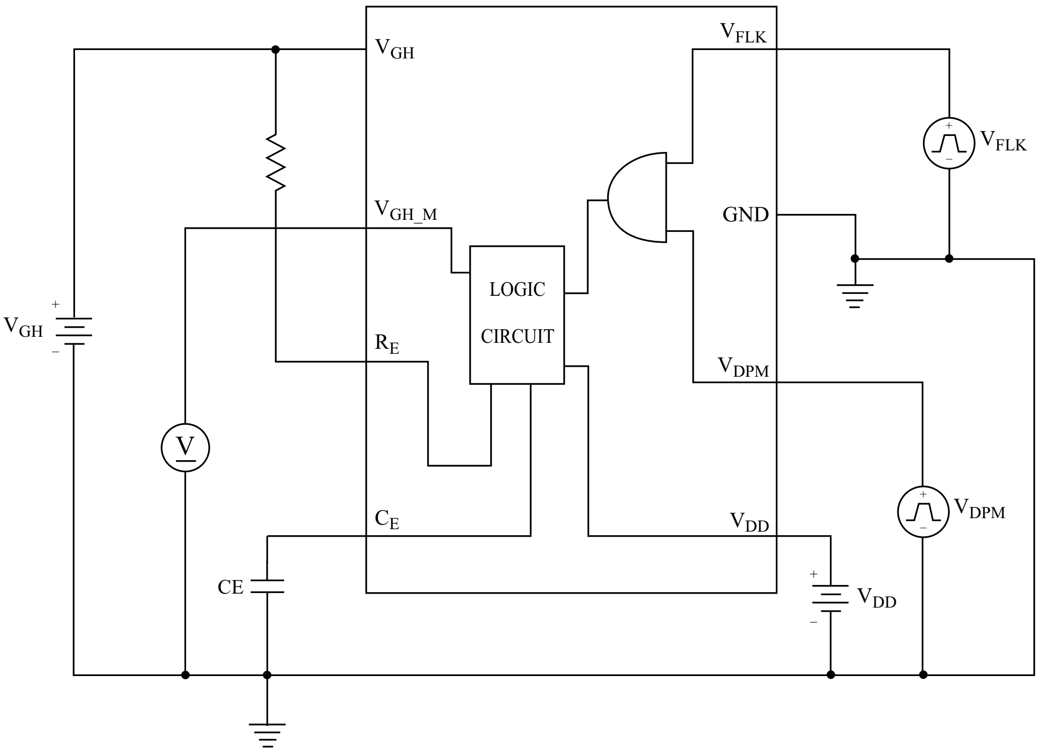
MARKING (US8 Package)



ELECTRICAL CHARACTERISTICS (V_{GH}=20V, V_{DD}=10V, V_{DPM}=2.2V, V_{FLK}=2.2V, V_{GH}-V_{DD} ≥ 8.5V Ta=25 ℃, Unless otherwise noted.)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Input	V_{GH}	V_{GH}-V_{DD} ≥8.5V	15	-	38	V
Reference Input	V_{DD}	V_{GH}-V_{DD} ≥8.5V	0	-	17	V
FLK High Voltage	$V_{FLK,H}$	V_{GH_M}=V_{GH}-1.2	2.2	-	3.6	V
FLK Low Voltage	$V_{FLK,L}$	V_{GH_M}=V_{DD}+1.5	0	-	0.5	V
DPM High Voltage	$V_{DPM,H}$	V_{FLK}=0V, V_{GH_M}=V_{DD} (Application 1,3)	2.2	-	3.6	V
DPM Low Voltage	$V_{DPM,L}$	V_{FLK}=0V, V_{GH_M} ≤0.6V (Application 1,3)	0	-	0.5	V
DPM on Current	I_{DPM}	V_{FLK}=3V, V_{GH_M}=V_{GH} (Application 2,3)	0.2	0.4	2	mA
RC (Resistor of V_{DPM} PIN)	R_C	V_{GH}=22V, R_C=(V_{GH}-0.9)/I_{DPM} (Application 2,3)	10	45	100	kΩ
Output High Voltage	$V_{GH\_M,H1}$	I_O=10mA	V_{GH}-1.2	V_{GH}-0.7	-	V
Output Reset Voltage	$V_{GH\_M,R1}$	V_{DPM}=0V, V_{FLK}=3V	-	-	0.6	V
	$V_{GH\_M,R2}$	V_{DPM}=0V, V_{FLK}=0V				
Output Low Voltage	$V_{GH\_M,L1}$	V_{DPM}=3V, V_{FLK}=0V, I_O=-1mA	V_{DD}	V_{DD}+0.7	V_{DD}+1.5	V9

● BLOCK DIAGRAM &TEST CIRCUIT



PIN CONNECTION

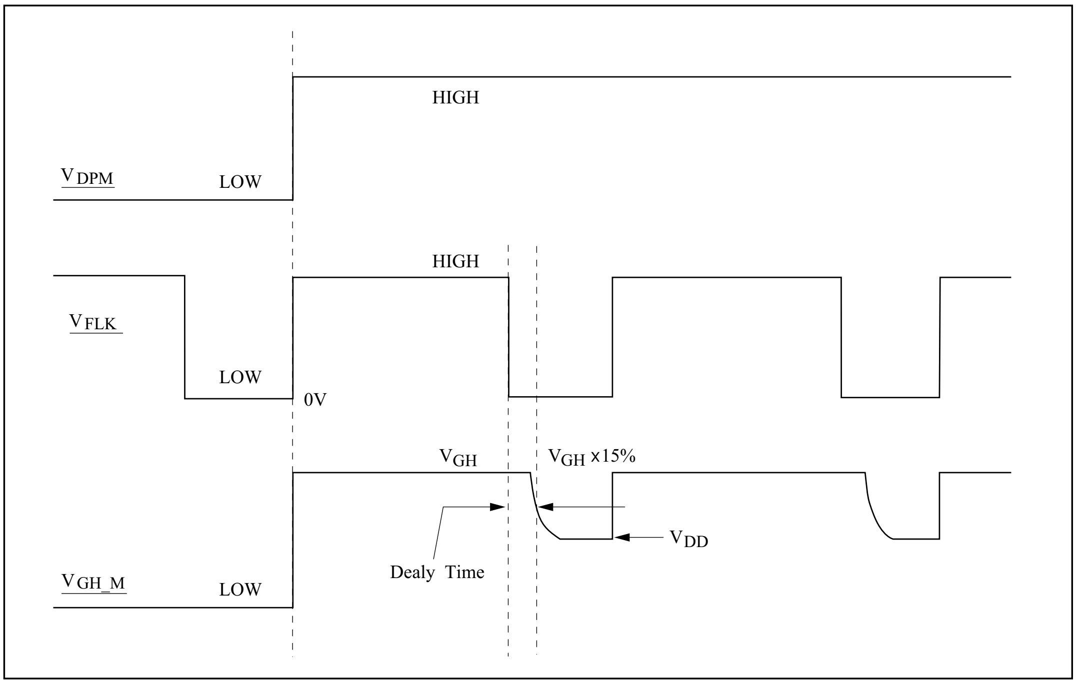
Pin No	1	2	3	4	5	6	7	8
KIA3820F	C_E	R_E	V_{GH_M}	V_{GH}	V_{FLK}	GND	V_{DPM}	V_{DD}
KIA3820FK	V_{GH}	V_{GH_M}	R_E	C_E	V_{DD}	V_{DPM}	GND	V_{FLK}

PIN FUNCTION DESCRIPTION

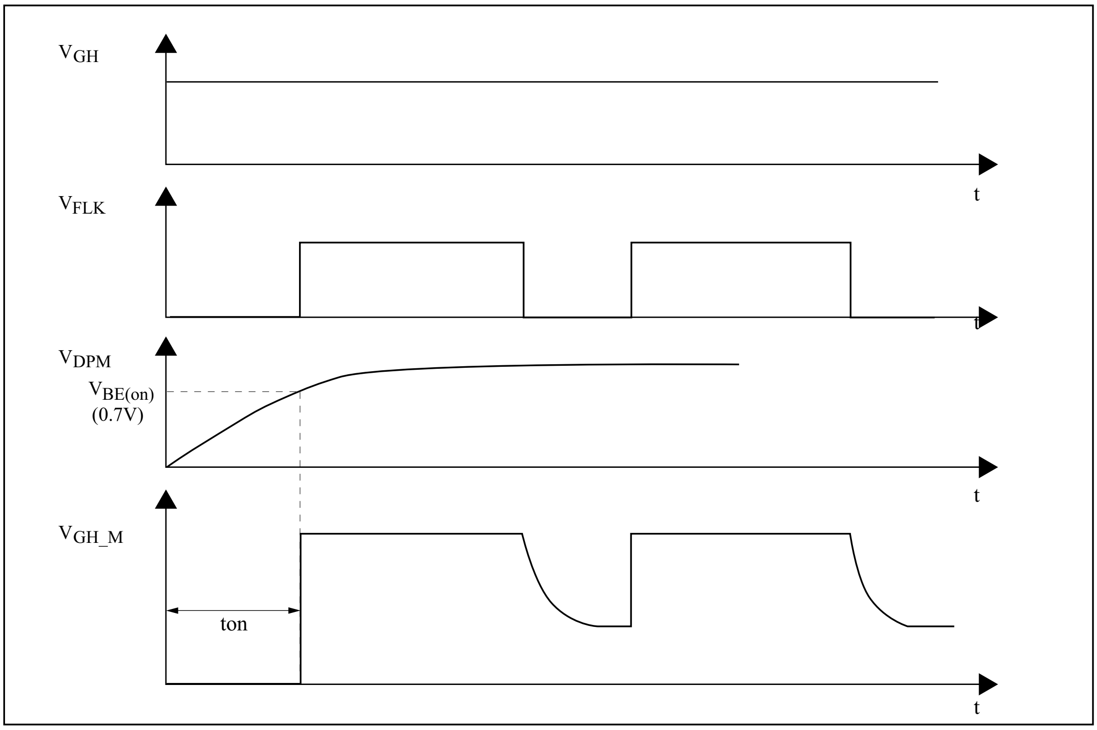
Pin Number (Note)	Pin Name	Pin Function	Comment
1/4	V_{GH}	Power Supply Input	V_{GH}=15~38V
2/3	V_{GH_M}	Output	This output directly drives the power supply of Gate Driver IC
3/2	R_E	R_E pin used to decide delay time	The Delay time are programmed by connecting resistor R_E to V_{GH} and capacitor C_E to ground
4/1	C_E	C_E Pin used decide delay time	
5/8	V_{DD}	Reference Input	The reference input Pin used to reduce flicker The Reference input voltage is as follows ; $V_{DD} \leq V_{GH}$-8.5V, V_{DD}=0~17V
6/7	V_{DPM}	Signal Input 1	V_{DPM} Single input voltage is as follows ; V_{DPM}=0~3.6V V_{DPM} pin is used to prevent situation which V_{GH}, V_{GL}, V_{CC} emerging from dc/dc converter is latched up, is produced from timing controller in LCD module, determines a time which V_{GH} is on.
7/6	GND	Ground	-
8/5	V_{FLK}	Signal Input 2	V_{FLK} Single input voltage is as follows ; V_{FLK}=0~3.6V V_{FLK} determines a time which TFT LCD is on/off, is produced from timing controller in LCD module.

Note) KIA3820FK / KIA3820F

• Input & Output Characteristics Graph (Application 1)

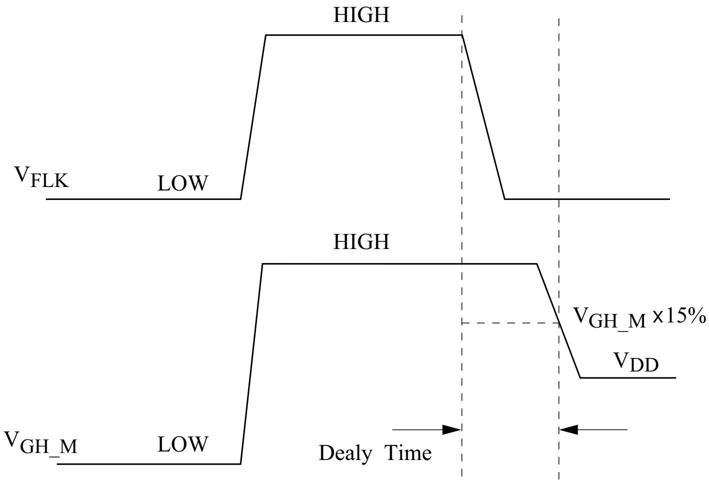


- **Input & Output Characteristics Graph (Application 2)**



- **. Definition of Delay Time**

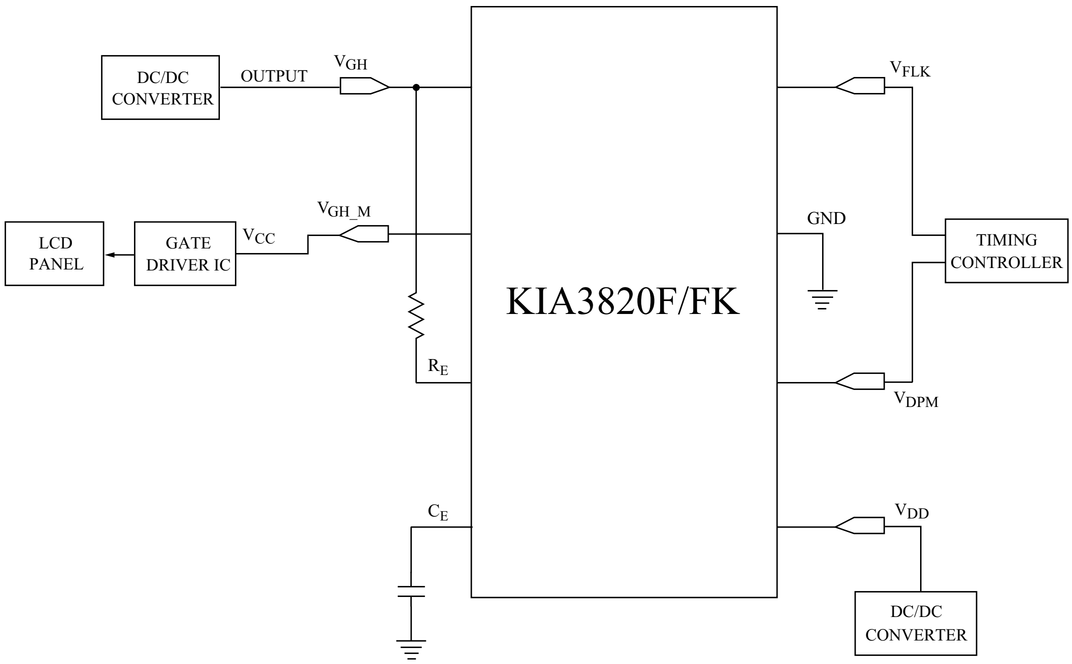
· Delay time is defined as the value of V_{GH_M} is falling to 15% of that after V_{FLK} is falling to the low.



- **Delay Time Characteristics Table.** (Unless otherwise specifies, V_{DPM}=3V, V_{FLK}=3V, R_E=15kΩ, R_{Emax}<100kΩ)

ITEM	CONDITION	RESULT
Delay time	V_{GH}=17V, V_{DD}=6.7V, C_P=100pF	1.48 (㎲)
	V_{GH}=17V, V_{DD}=6.7V, C_P=240pF	3.08 (㎲)
	V_{GH}=22.4V, V_{DD}=10V, C_P=92pF	1.54 (㎲)
	V_{GH}=22.4V, V_{DD}=10V, C_P=226pF	2.98 (㎲)
	V_{GH}=25.4V, V_{DD}=15.4V, C_P=56pF	1.50 (㎲)
	V_{GH}=25.4V, V_{DD}=15.4V, C_P=139pF	3.02 (㎲)

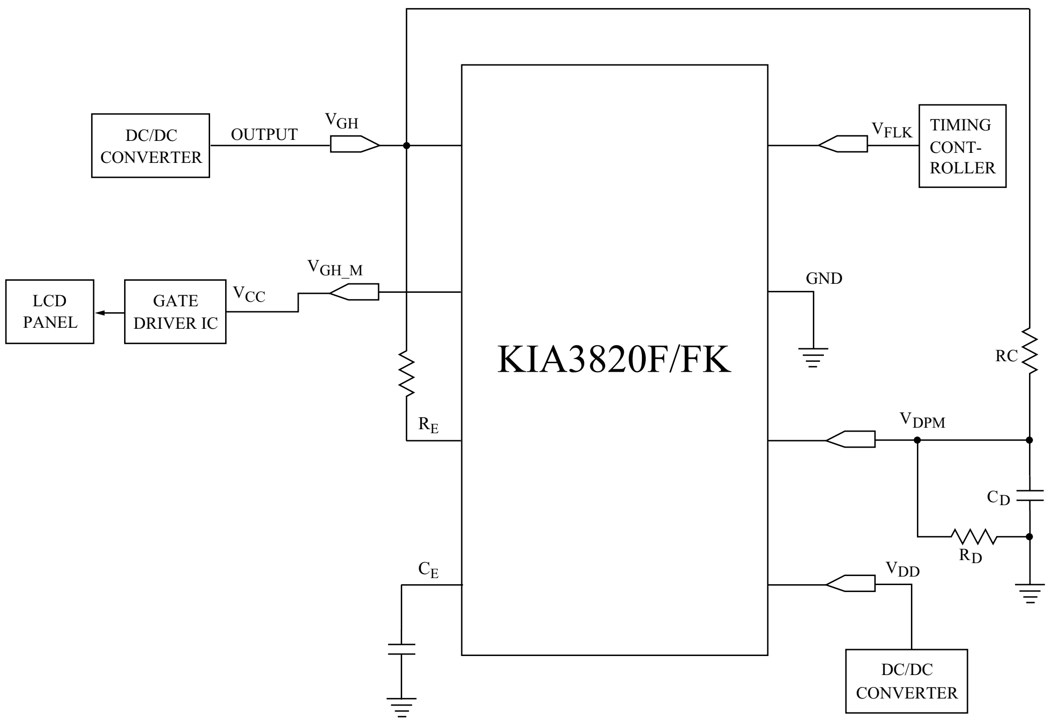
APPLICATION 1



APPLICATION 2

V_{DPM} signal is produced by connecting resistor R_C to V_{GH} and capacitor C_D to ground

R_D used to discharge when V_{GH} signal is low voltage.



• **V_{GH_M} Signal Delay Time Characteristics Table.**

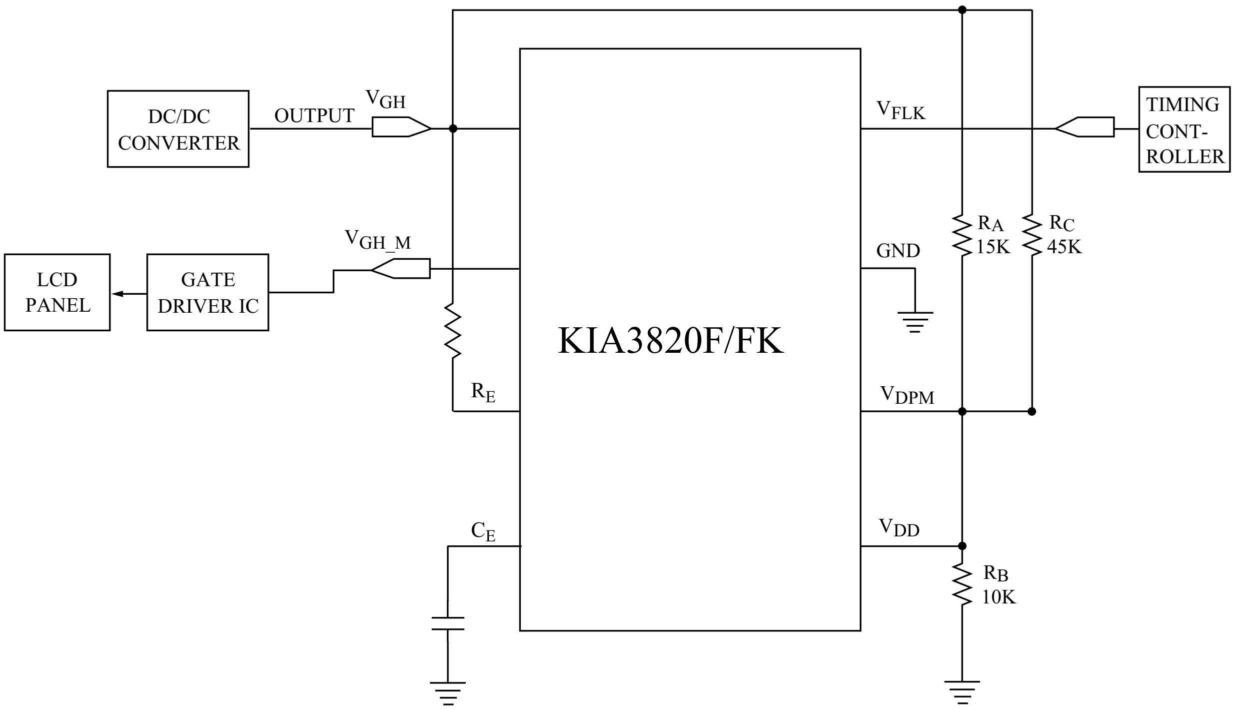
V_{GH} [V]	V_{DD} [V]	C_D [μF]	R_D [kΩ]	R_C [kΩ]	V_{GH_M} on delay time (when V_{GH} is on) ton (ms)	V_{DPM} pin discharge time (when V_{GH} is off) toff (ms)
22	12	1	2	50	3.4	4
		1	0.8	20	1.8	1.6
		1	0.4	10	1	0.8

• **Function Description**

name	Comment	Function
R_C	R_C & C_D determines a time which V_{DPM} pin is charge	t_{on} : The time which V_{GH_M} is high $t_{on} \fallingdotseq (0.14 \times C_D \times R_C \times C_D) / ((R_D \times (V_{GH}-0.7))-(0.7 \times R_C))$ $R_D \geqq R_C \times (0.9/(V_{GH}-0.9))$ t_{off} : The time which V_{DPM} pin is full discharge $t_{off} \fallingdotseq 2 \times R_D \times C_D$ $R_{Cmin} = (V_{GH}-0.9)/2mA$ $R_{Cmax} = (V_{GH}-0.9)/200\mu A$
C_D		
R_D	R_D determines a time which V_{DPM} pin is discharge	

APPLICATION 3

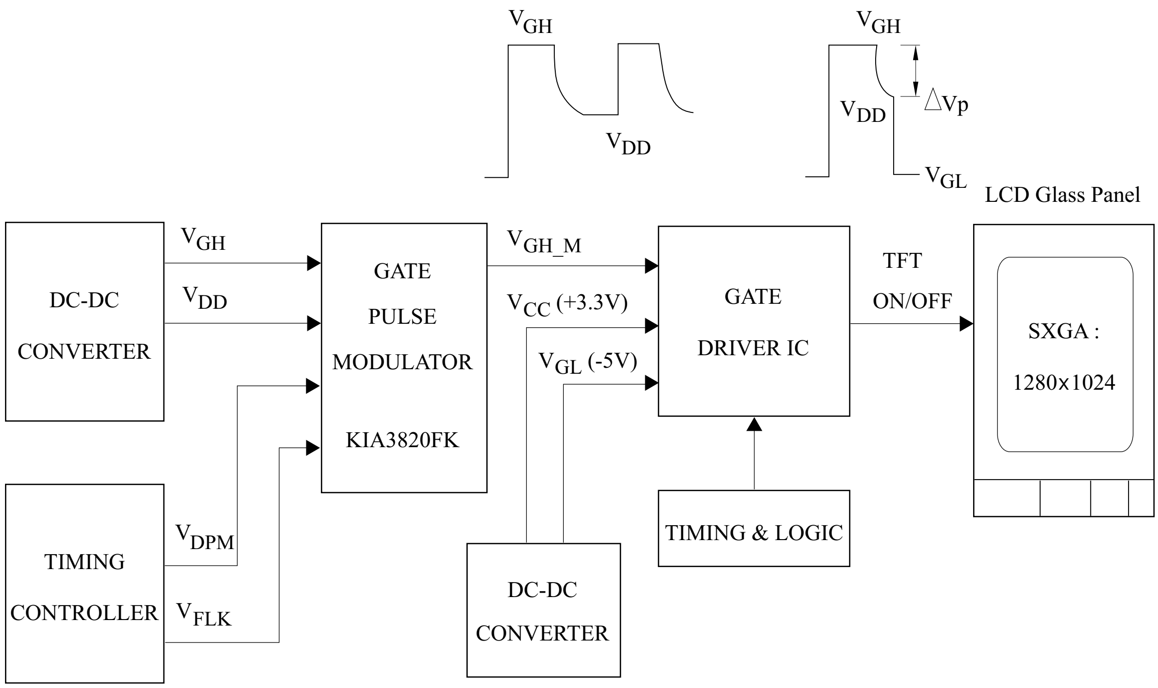
If there is no use to V_{DPM} termnal function which suggested in APPLICATION 1 and 2, USE the following APPLICATION3. Also, V_{DD} Voltage is possible to use Voltage which is divided V_{GH} Voltage, so we don't use to external power supply. This method is possible to apply APPLICATION 1 and 2.



• Function Description

name	Comment	Function
R_A	R_A & RB determines a V_{DD} Voltage.	$V_{DD}=V_{GH} \times (R_B/(R_A+R_B))$
R_B		
R_C	R_C is used to determines Voltage that V_{DPM} pin becomes high	$(V_{GH} - 0.9) / 2mA) < R_C < ((V_{GH} - 0.9) / 0.2mA)$

● APPLICATION SYSTEM BLOCK DIAGRAM



note) △Vp is decreasing more and more, Flick is reduced from LCD panel