



## ESD Protection Arrays, Chip Scale Package

### Features

- 4, 8, or 16 transient voltage suppressors in a single package
- In-system Electrostatic Discharge (ESD) protection to 25kV contact discharge per IEC 61000-4-2 international standard
- Compact Chip Scale Package (0.65mm pitch) format saves board space and eases layout in space critical applications compared to discrete solutions and traditional wire bonded packages

### Applications

- ESD protection of I/O port connections, such as cellular phone, PDA, internet appliance and PC ports
- Protection of interface ports or IC pins which are exposed to high levels of ESD

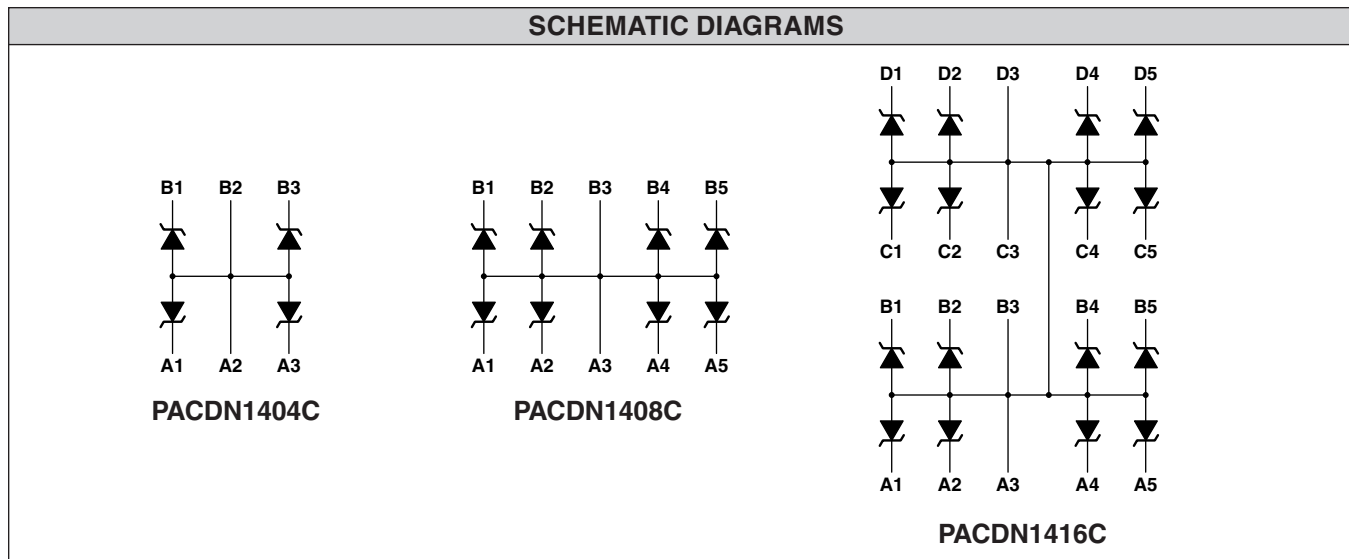
### Product Description

The PACDN1404C, PACDN1408C and PACDN1416C are transient voltage suppressor arrays that provide a very high level of protection for sensitive electronic components that may be subjected to ESD.

These devices are designed and characterized to safely dissipate ESD strikes at levels well beyond the maximum requirements set forth in the IEC 61000-4-2 international standard (Level 4, 8kV contact discharge). All I/Os are rated at 25kV using the IEC 61000-4-2 contact discharge method. Using the MIL-STD-883D

(Method 3015) specification for Human Body Model (HBM) ESD, all pins are protected for contact discharges to greater than 30kV.

The Chip Scale Package format of these devices enable extremely small footprints that are necessary in portable electronics such as cellular phones, PDAs, internet appliances and PCs. The large solder bumps allow for standard attachment to laminate boards without the use of underfill.



| STANDARD PART ORDERING INFORMATION |       |                      |  |
|------------------------------------|-------|----------------------|--|
| Package                            |       | Ordering Part Number |  |
| Style                              | Bumps | Tape & Reel          |  |
| Chip Scale                         | 6     | PACDN1404C/R         |  |
| Chip Scale                         | 10    | PACDN1408C/R         |  |
| Chip Scale                         | 20    | PACDN1416C/R         |  |

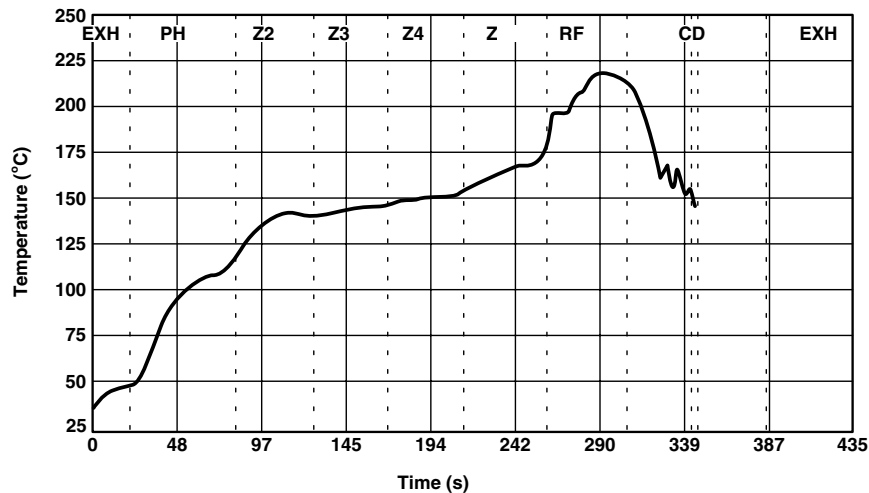


| SPECIFICATIONS<br>(At 25°C unless specified otherwise) |      |      |      |      |
|--|------|------|------|------|
|  | Min  | Typ  | Max  | Unit |
| Reverse Stand-off Voltage, I = 10µA                    | 5.5  |      |      | V    |
| Signal Clamp Voltage:                                  |      |      |      |      |
| Positive Clamp, 10mA                                   | 5.6  | 6.6  | 8.0  | V    |
| Negative Clamp, 10mA                                   | -1.2 | -0.8 | -0.4 | V    |
| In-system ESD withstand voltage*:                      |      |      |      |      |
| Human Body Model (MIL-STD-883D, method 3015)           |      | ±30  |      | kV   |
| IEC 61000-4-2, contact discharge method                |      | ±25  |      | kV   |
| Clamping voltage during ESD discharge                  |      | 12   |      | V    |
| MIL-STD-883D (Method 3015), 8kV                        |      | -8   |      | V    |
| Capacitance at 2.5V dc, 1MHz                           |      | 39   |      | pF   |
| Temperature Range:                                     |      |      |      |      |
| Operating  | -40  |      | 85   | °C   |
| Storage  | -65  |      | 150  |      |

\* ESD applied between channel pin and ground, one at a time. All other channels are open. All GND pins grounded. This parameter is guaranteed by design and characterization.

'GND' in this document refers to the lower supply voltage.

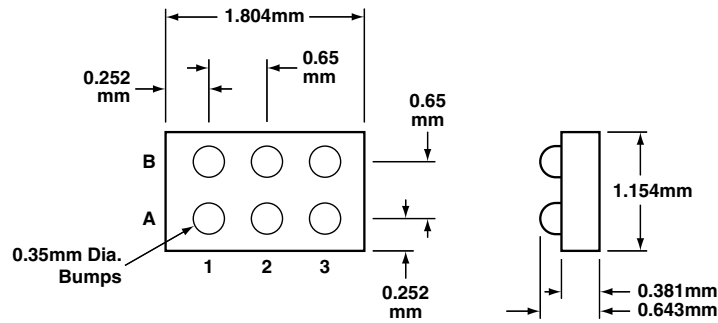
| PRINTED CIRCUIT BOARD RECOMMENDATIONS |                                     |
|---------------------------------------|-------------------------------------|
| Pad Size on PCB                       | 0.300mm                             |
| Pad Shape                             | Round                               |
| Pad Definition                        | Non Solder Mask Defined Pads (NSMD) |
| Solder Mask Opening                   | 0.350mm                             |
| Solder Stencil Thickness              | 0.152mm                             |
| Solder Stencil Aperture Opening       | 0.360mm (sq.)                       |
| Solder Flux Ratio                     | 50/50                               |
| Solder Paste                          | No Clean                            |
| Bond Trace Finish                     | OSP (Entek Cu Plus 106A)            |



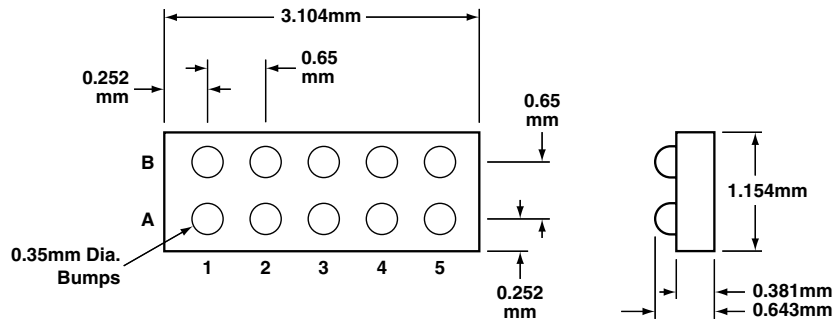
Typical Solder Reflow Thermal Profile (No Clean Flux)



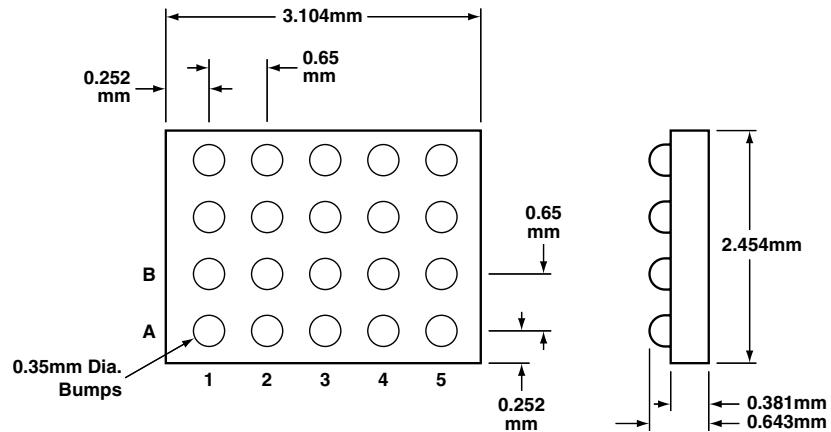
### Package Diagrams



PACDN1404C



PACDN1408C



PACDN1416C

### Pin Orientation

Components are symmetrical, and do not require orientation to pin-1 found in conventional semiconductors. The part may be rotated 180° without affecting operation.