

# FDG312P

## P-Channel 2.5V Specified PowerTrench™ MOSFET

### General Description

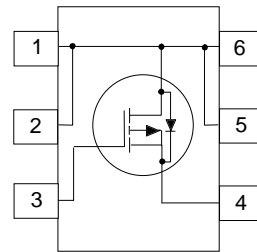
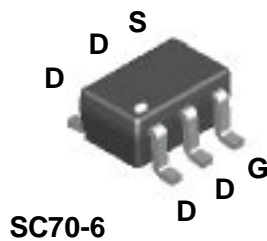
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.

### Applications

- Load switch
- Battery protection
- Power management

### Features

- -1.2 A, -20 V.  $R_{DS(on)} = 0.18 \Omega @ V_{GS} = -4.5 V$   
 $R_{DS(on)} = 0.25 \Omega @ V_{GS} = -2.5 V.$
- Low gate charge (3.3 nC typical).
- High performance trench technology for extremely low  $R_{DS(on)}$ .
- Compact industry standard SC70-6 surface mount package.



### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	± 8	V
I <sub>D</sub>	Drain Current - Continuous (Note 1)	-1.2	A
		-6	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	0.75	W
	(Note 1b)	0.55	
	(Note 1c)	0.48	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1)	260	°C/W
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### Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.12	FDG312P	7"	8mm	3000 units

## DMOS Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-19		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		2.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -1.2\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.2\text{ A}$ @ $125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.135 0.200 0.187	0.18 0.29 0.25	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-3			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -1.2\text{ A}$		3.8		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		330		pF
$C_{oss}$	Output Capacitance			80		pF
$C_{rss}$	Reverse Transfer Capacitance			35		pF

### Switching Characteristics (Note 2)

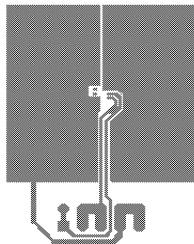
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -5\text{ V}, I_D = -0.5\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		7	15	ns
$t_r$	Turn-On Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			16	26	ns
$t_f$	Turn-Off Fall Time			5	12	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -1.2\text{ A},$ $V_{GS} = -4.5\text{ V}$		3.3	5	nC
$Q_{gs}$	Gate-Source Charge			0.8		nC
$Q_{gd}$	Gate-Drain Charge			0.7		nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-0.6	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.6\text{ A}$ (Note 2)		-0.83	-1.2	V

#### Notes:

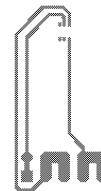
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $170^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz copper.



b)  $225^\circ\text{C/W}$  when mounted on a half of package sized 2oz copper.



c)  $260^\circ\text{C/W}$  when mounted on a minimum pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

### Typical Characteristics

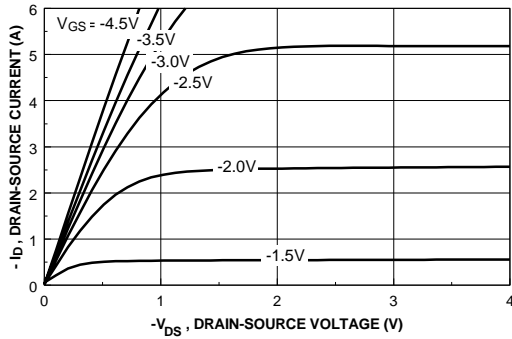


Figure 1. On-Region Characteristics.

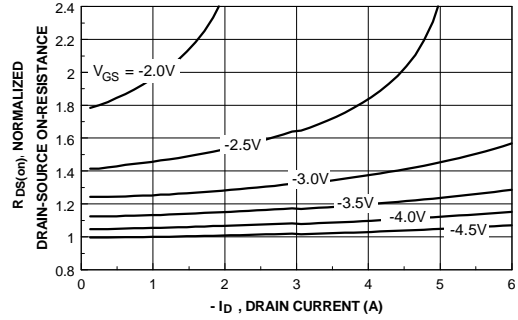


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

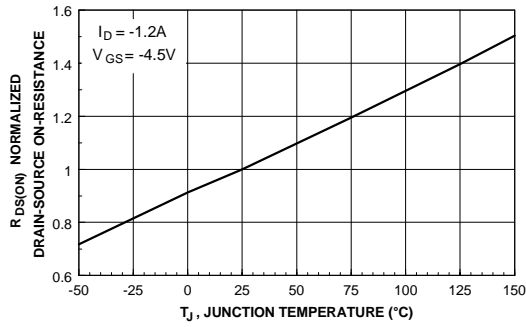


Figure 3. On-Resistance Variation with Temperature.

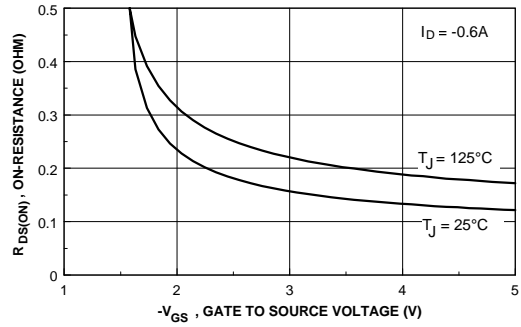


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

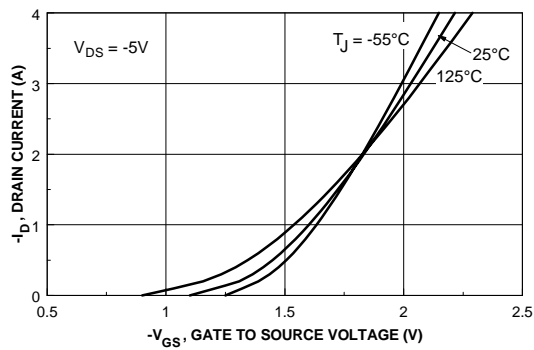


Figure 5. Transfer Characteristics.

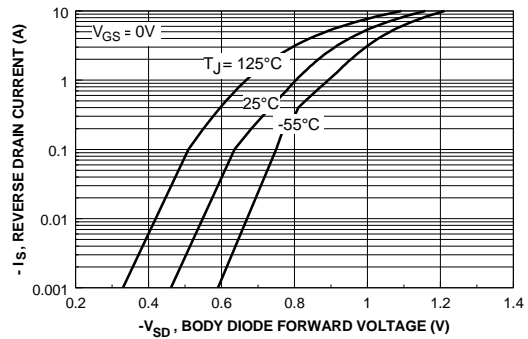


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

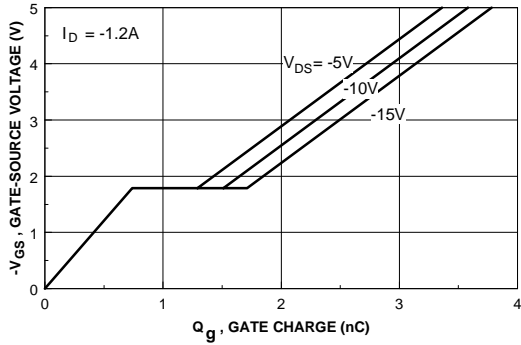


Figure 7. Gate-Charge Characteristics.

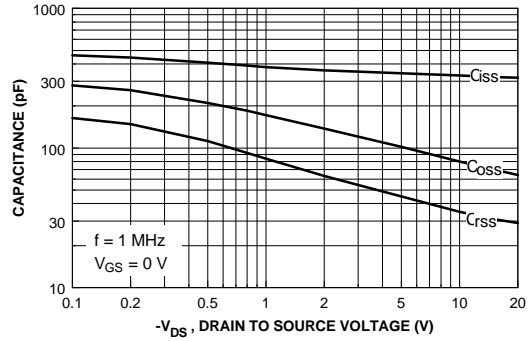


Figure 8. Capacitance Characteristics.

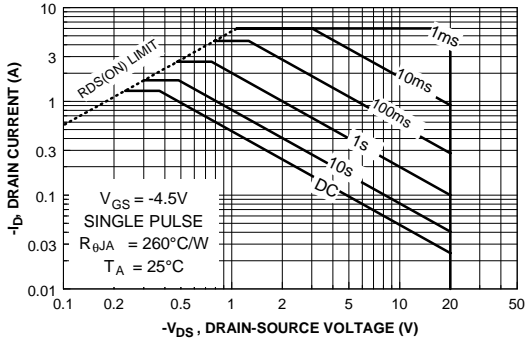


Figure 9. Maximum Safe Operating Area.

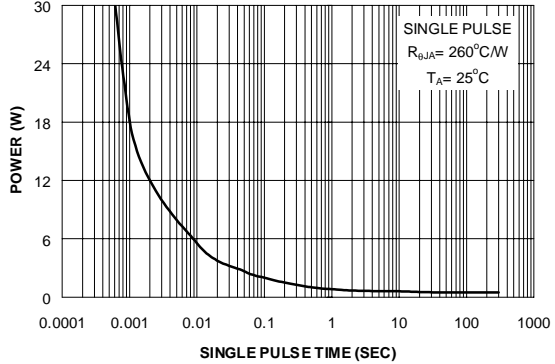


Figure 10. Single Pulse Maximum Power Dissipation.

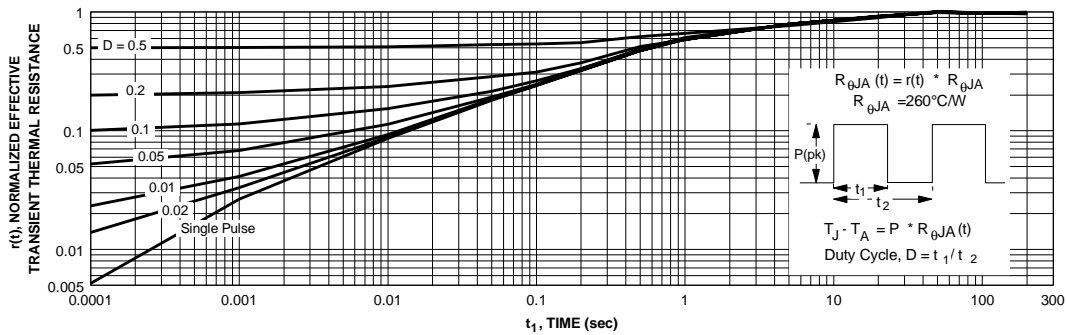


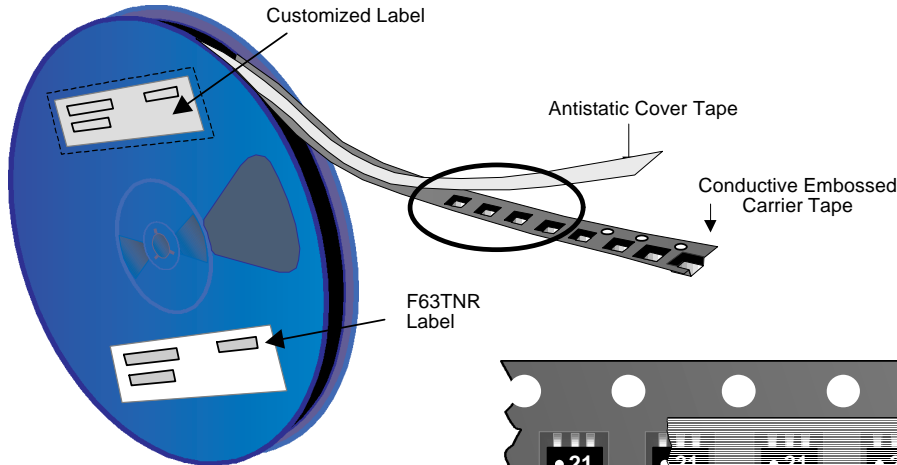
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

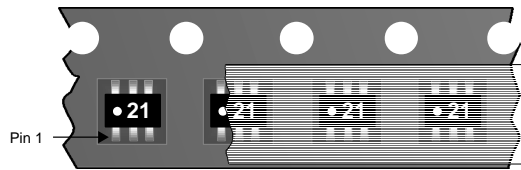
# SC70-6 Tape and Reel Data and Package Dimensions



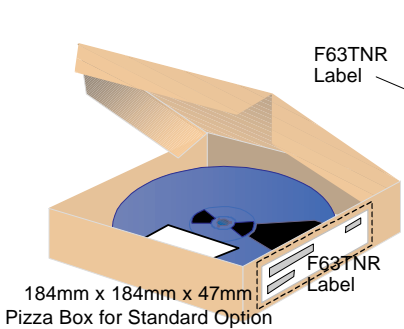
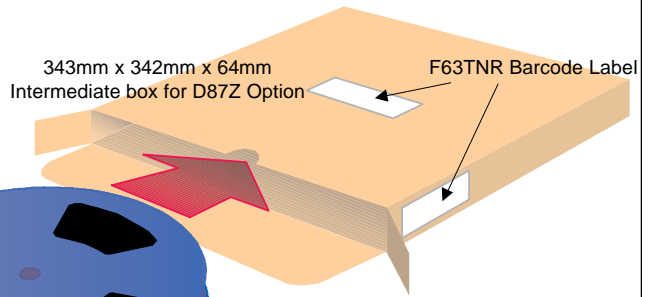
## SC70-6 Packaging Configuration: Figure 1.0



SC70-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	184x187x47	343x343x64
Max qty per Box	9,000	20,000
Weight per unit (gm)	0.0055	0.0055
Weight per Reel (kg)	0.1140	0.3960
Note/Comments		



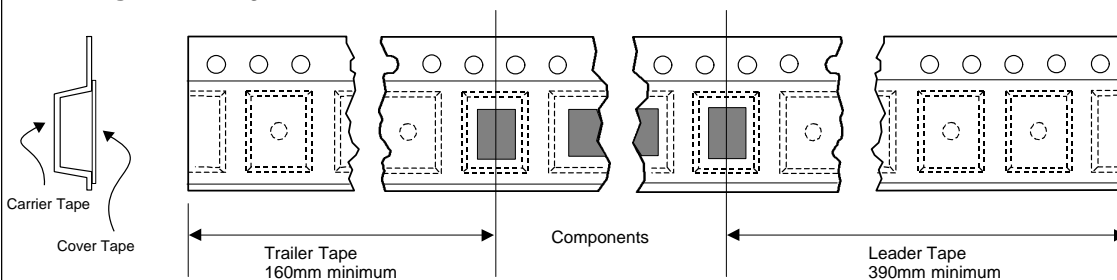
SC70-6 Unit Orientation



F63TNR Label sample

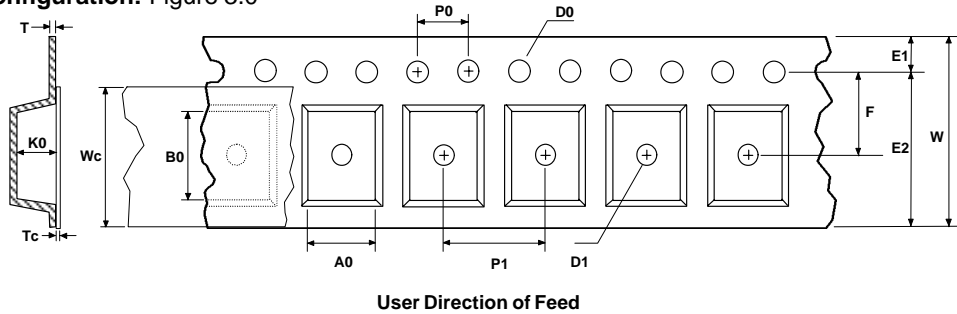


## SC70-6 Tape Leader and Trailer Configuration: Figure 2.0



# SC70-6 Tape and Reel Data and Package Dimensions, continued

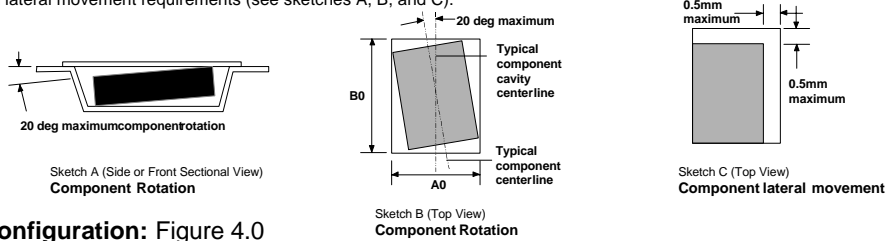
## SC70-6 Embossed Carrier Tape Configuration: Figure 3.0



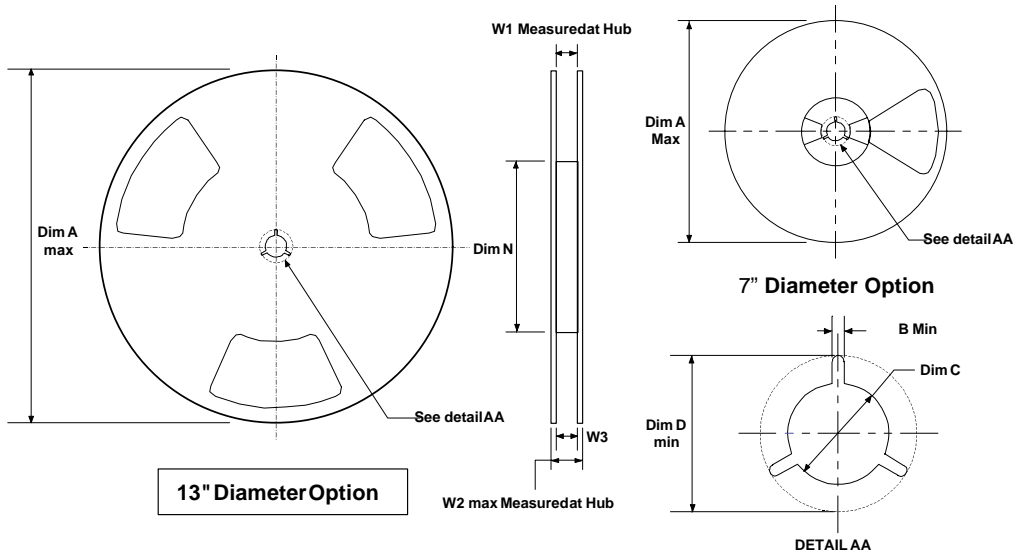
User Direction of Feed

Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SC70-6 (8mm)	3.24 +/-0.10	2.34 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.00 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.20 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



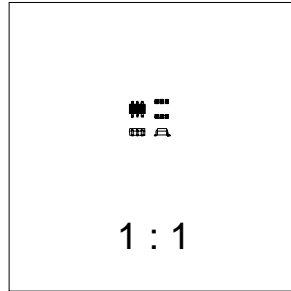
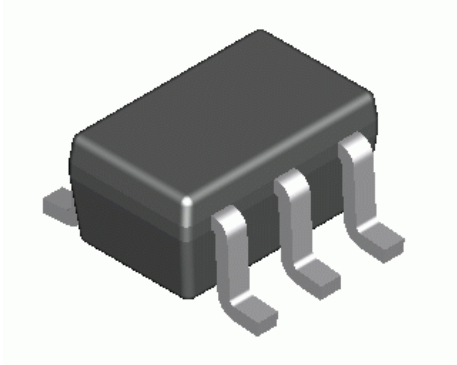
## SC70-6 Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

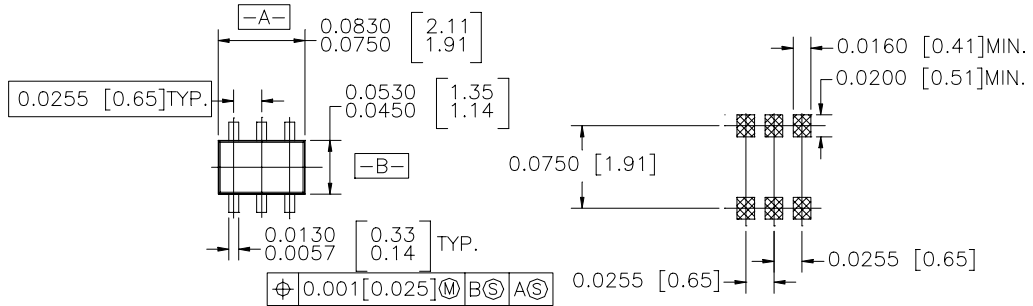
**SC70-6 Tape and Reel Data and Package Dimensions, continued**

**SC70-6 (FS PKG Code 76)**

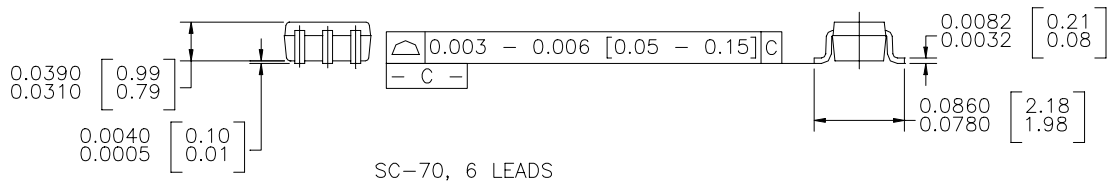


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Part Weight per unit (gram): 0.0055



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E <sup>2</sup> CMOS™	PowerTrench®	VCX™
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

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