

MOS FIELD EFFECT POWER TRANSISTORS 2SJ324, 2SJ324-Z

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ324 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low On-state Resistance

RDS(on) = 0.18
$$\Omega$$
 TYP. (VGS = -10 V, ID = -1 A)
RDS(on) = 0.36 Ω TYP. (VGS = -4 V, ID = -0.8 A)

- Low Ciss Ciss = 330 pF TYP.
- Built-in G-S Gate Protection Diode

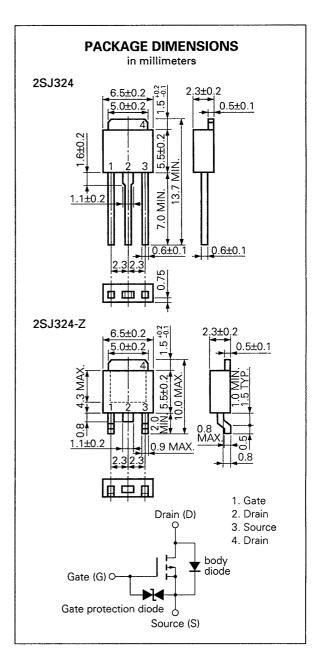
QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Drain to Source Voltage	VDSS	-30	٧
Gate to Source Voltage (AC)	Vgss	∓20	٧
Gate to Source Voltage (DC)	Vgss	-20, +10	٧
Drain Current (DC)	ÎD(DC)	∓2.0	Α
Drain Current (pulse)	ID(pulse)*	∓8.0	Α
Total Power Dissipation ($T_c = 25$ °C)	P _{T1}	20	W
Total Power Dissipation (Ta = 25 °C)	PT2	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
* PW \leq 10 μ s, Duty Cycle \leq 1 %			

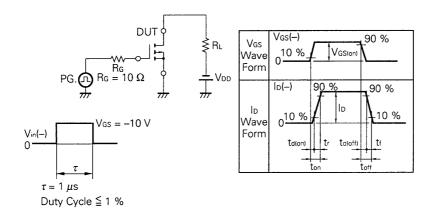




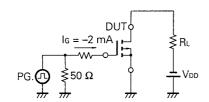
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	RDS(on)		0.18	0.25	Ω	Vgs = -10 V, Io = -1.0 A
Drain to Source On-state Resistance	RDS(on)		0.36	0.52	Ω	Vgs = -4 V, ID = -0.8 A
Gate to Source Cutoff Voltage	VGS(off)	-1.0	-1.5	-2.0	٧	Vps = -10 V, lp = -1 mA
Forward Transfer Admittance	yfs	1.0	1.9		S	V _{DS} = -10 V, I _D = -1.0 A
Drain Leakage Current	loss			-10	μΑ	Vps = -30 V, Vgs = 0
Gate to Source Leakage Current	lgss			±10	μΑ	Vgs = ∓16 V, Vps = 0
Input Capacitance	Ciss		330		pF	V _{DS} = -10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	Coss		290		pF	
Reverse Transfer Capacitance	Crss		105		pF	
Turn-On Delay Time	td(on)		7		ns	$V_{GS(on)} = -10 \text{ V}$ $V_{DD} = -15 \text{ V}$ $I_{D} = -1.0 \text{ A, Rg} = 10 \Omega$ $R_{L} = 15 \Omega$
Rise Time	tr		35		ns	
Turn-Off Delay Time	td(off)		40		ns	
Fall Time	tf		30		ns	
Total Gate Charge	Q _G		12		nC	V _{GS} = -10 V I _D = -2.0 A V _{DD} = -24 V
Gate to Source Charge	Qgs		1.5		nC	
Gate to Drain Charge	Q _{GD}		4.5		nC	
Body Diode Forward Voltage	VF		0.9		V	IF = 2.0 A, Vgs = 0
Reverse Recovery Time	trr		50		ns	I _F = 2.0 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Qrr		40		nC	
ESD	VESD		±130		٧	C = 200 pF, R = 0, Single Pulse

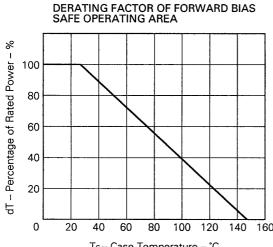
Test Circuit 1: Switching Time

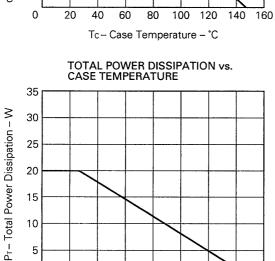


Test Circuit 2: Gate Charge



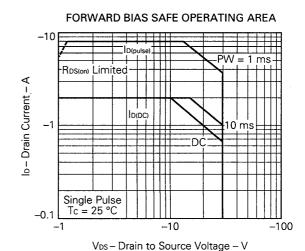
TYPICAL CHARACTERISTICS (Ta = 25 °C)

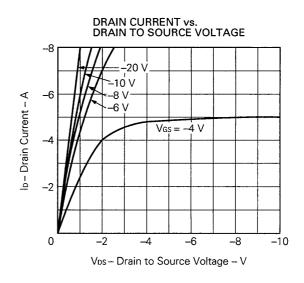


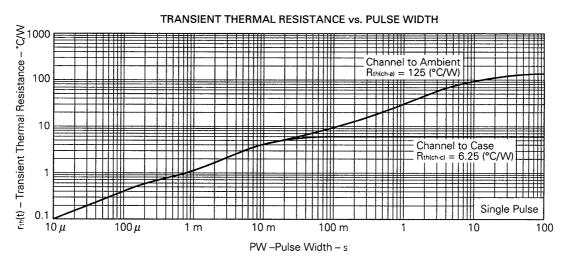


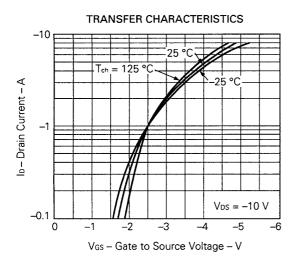
140 160

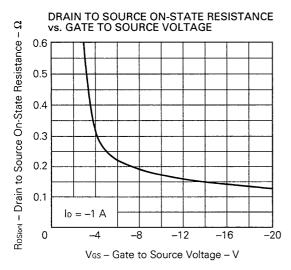
Tc - Case Temperature - °C

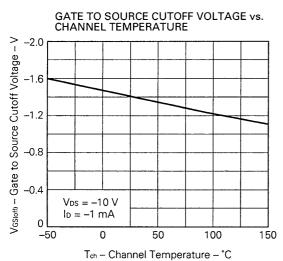




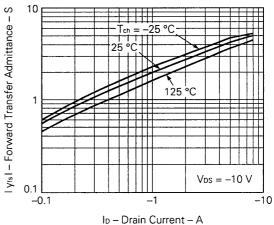




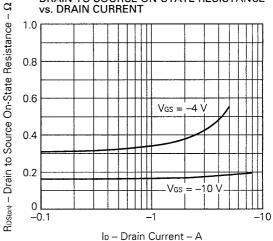




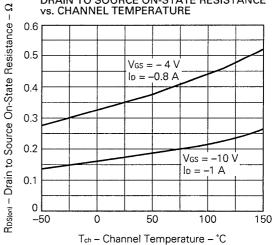


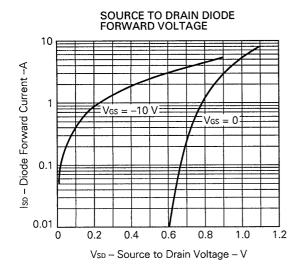


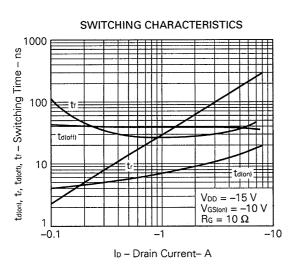
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

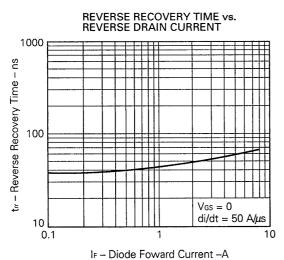


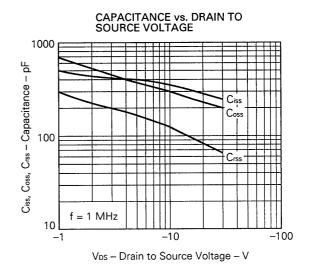
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

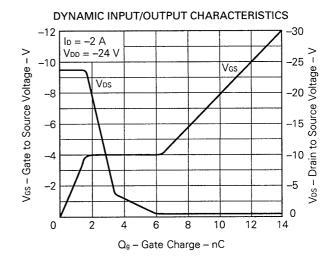












Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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