

HAT1047R, HAT1047RJ

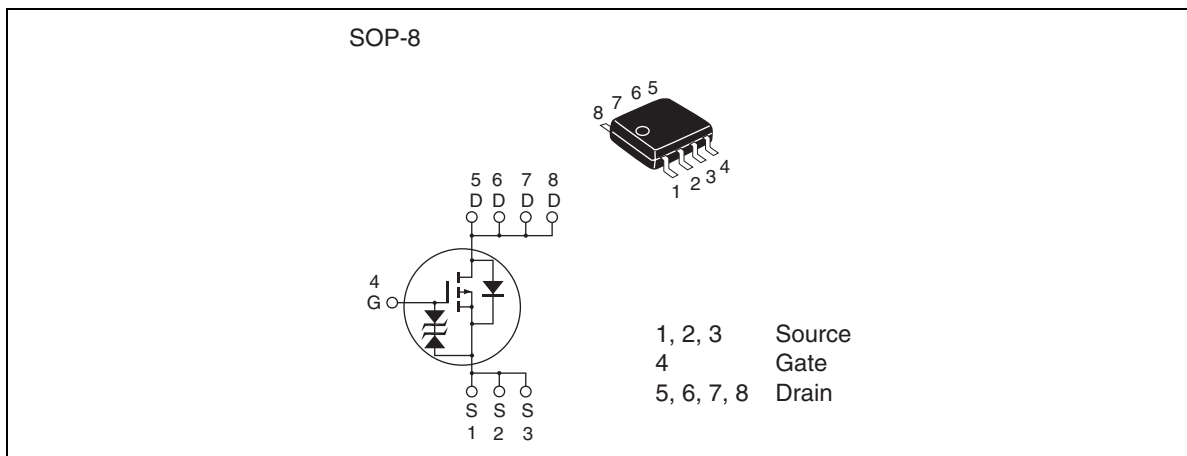
Silicon P Channel Power MOS FET
High Speed Power Switching

REJ03G0074-0500Z
(Previous ADE-208-1545D(Z))
Rev.5.00
Aug.27.2003

Features

- For Automotive Application (at Type Code "J")
- Low on-resistance
- Capable of -4.5 V gate drive
- High density mounting

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-14	A
Drain peak current	I _{D(pulse)} ^{Note1}	-112	A
Body-drain diode reverse drain current	I _{DR}	-14	A
Avalanche current	HAT1047R	I _{AP} ^{Note3}	—
	HAT1047RJ		-14
Avalanche energy	HAT1047R	E _{AR} ^{Note3}	—
	HAT1047RJ		19.6
Channel dissipation	P _{ch} ^{Note2}	2.5	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1 %
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s
3. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

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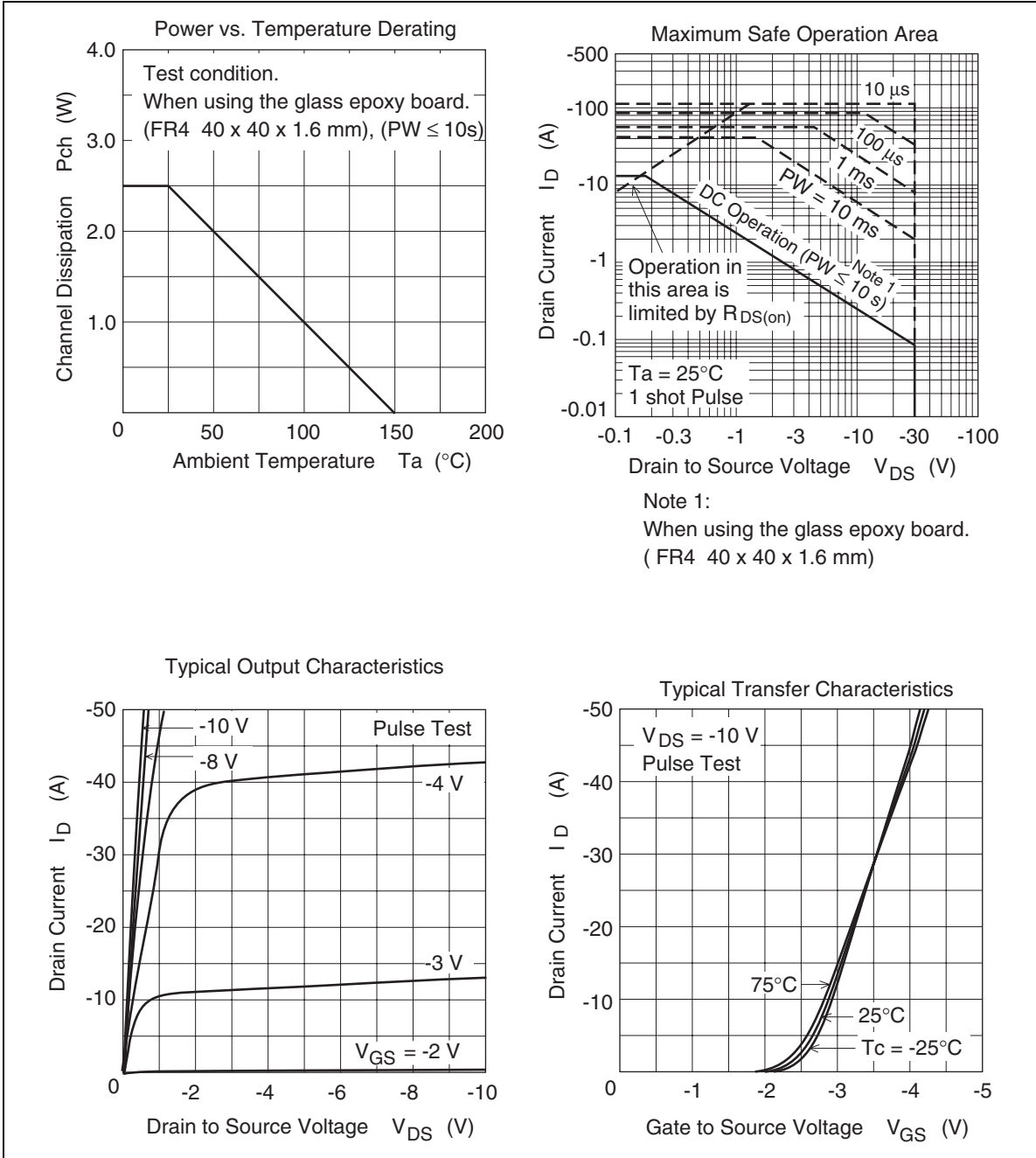
Electrical Characteristics

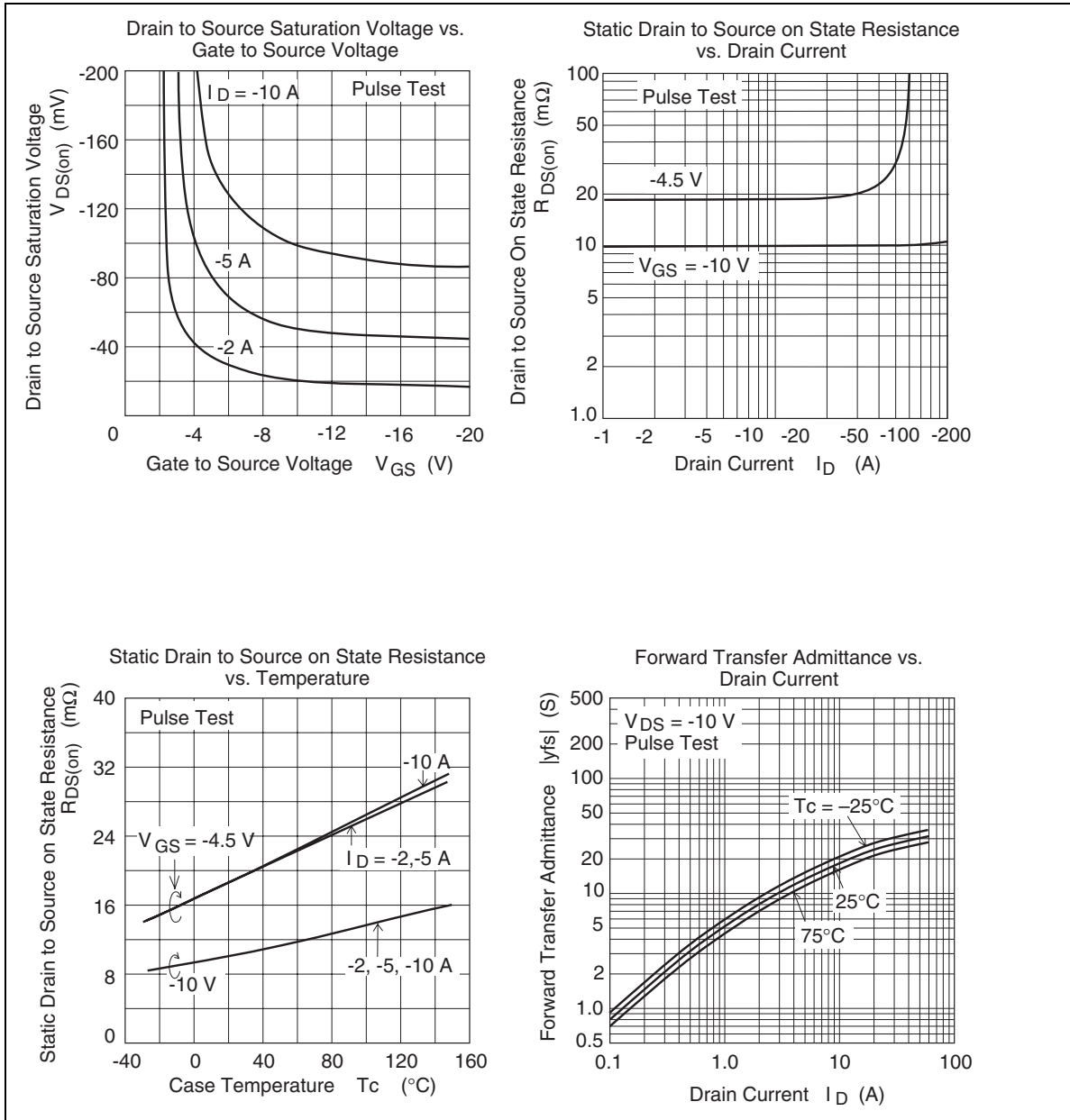
(Ta = 25°C)

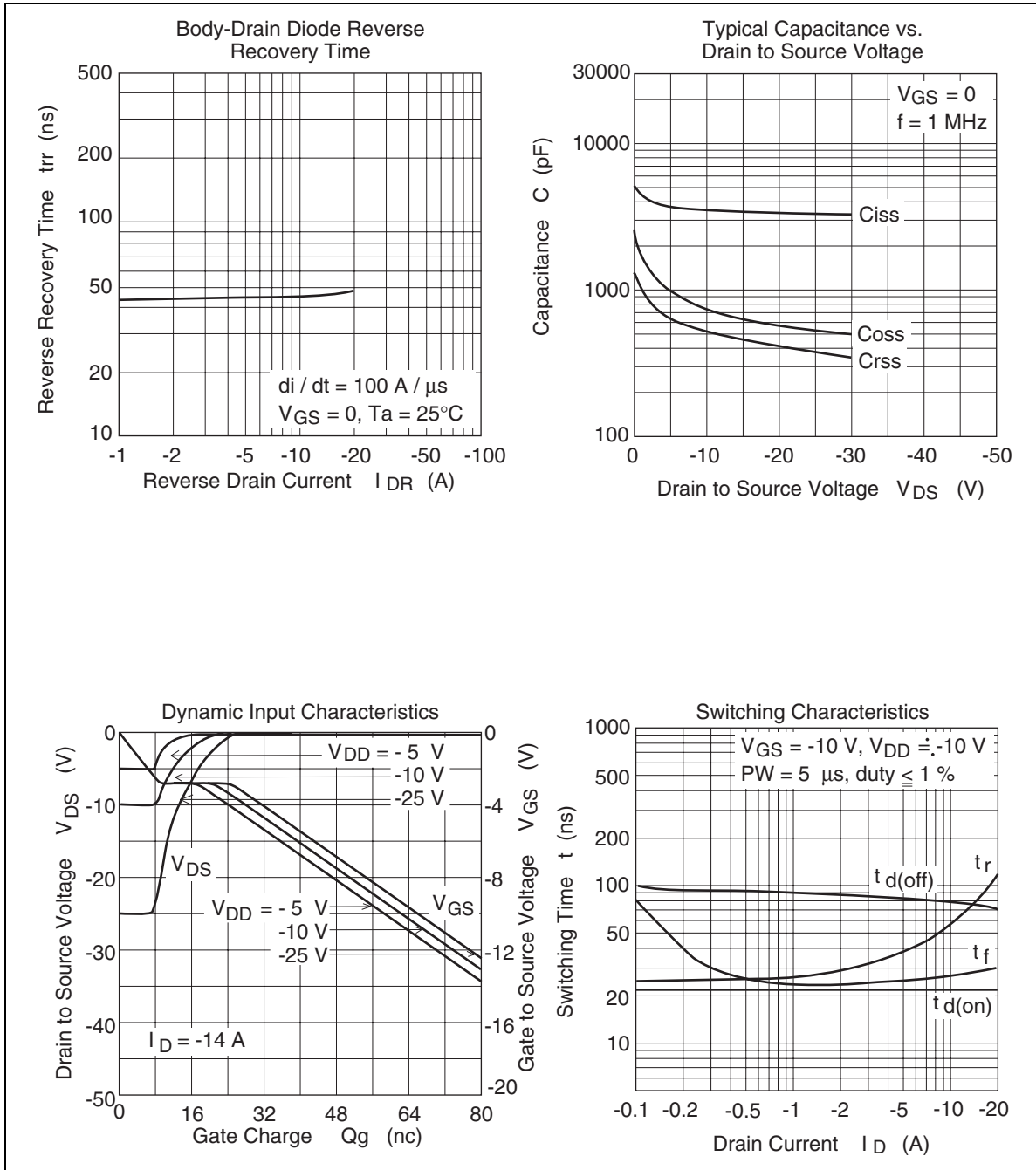
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	mV	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	± 1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Zero gate voltage drain current	HAT1047R I_{DSS}	—	—	—	μA	$V_{DS} = -24 \text{ V}$, $V_{GS} = 0$
drain current	HAT1047RJ I_{DSS}	—	—	-20	μA	Ta = 125°C
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	10	12	m Ω	$I_D = -7 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	19	25	m Ω	$I_D = -7 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	9.6	16	—	S	$I_D = -7 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	3500	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	750	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	520	—	pF	f = 1 MHz
Total gate charge	Q_g	—	64	—	nc	$V_{DD} = -10 \text{ V}$
Gate to source charge	Q_{gs}	—	10	—	nc	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Q_{gd}	—	12	—	nc	$I_D = -14 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -7\text{A}$
Rise time	t_r	—	45	—	ns	$V_{DD} \cong -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	$R_L = 1.43 \text{ }\Omega$
Fall time	t_f	—	25	—	ns	$R_L = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	-0.82	-1.07	V	$I_F = -14 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = -14 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

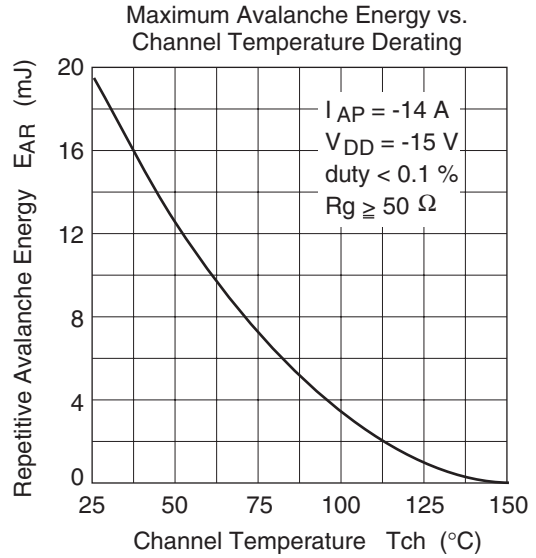
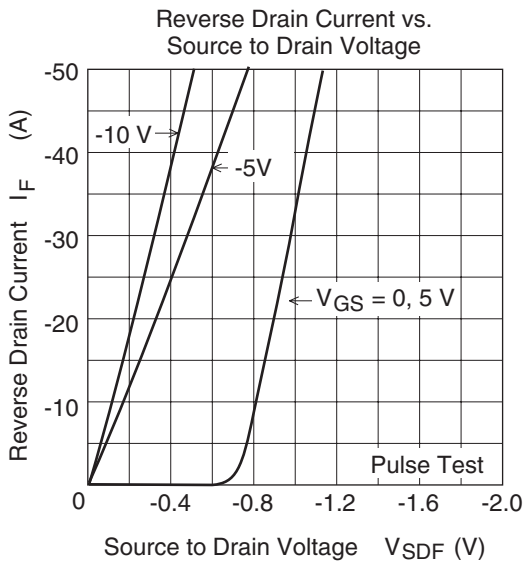
Notes: 4. Pulse test

Main Characteristics

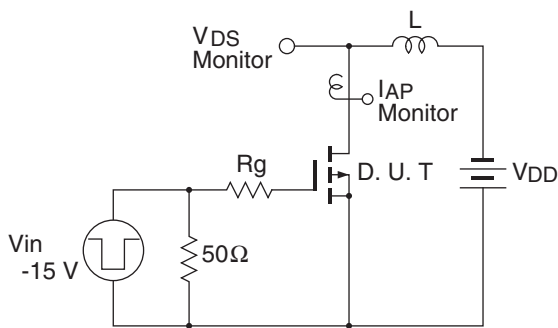




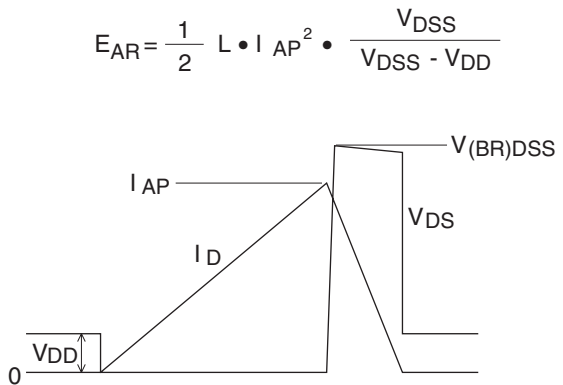


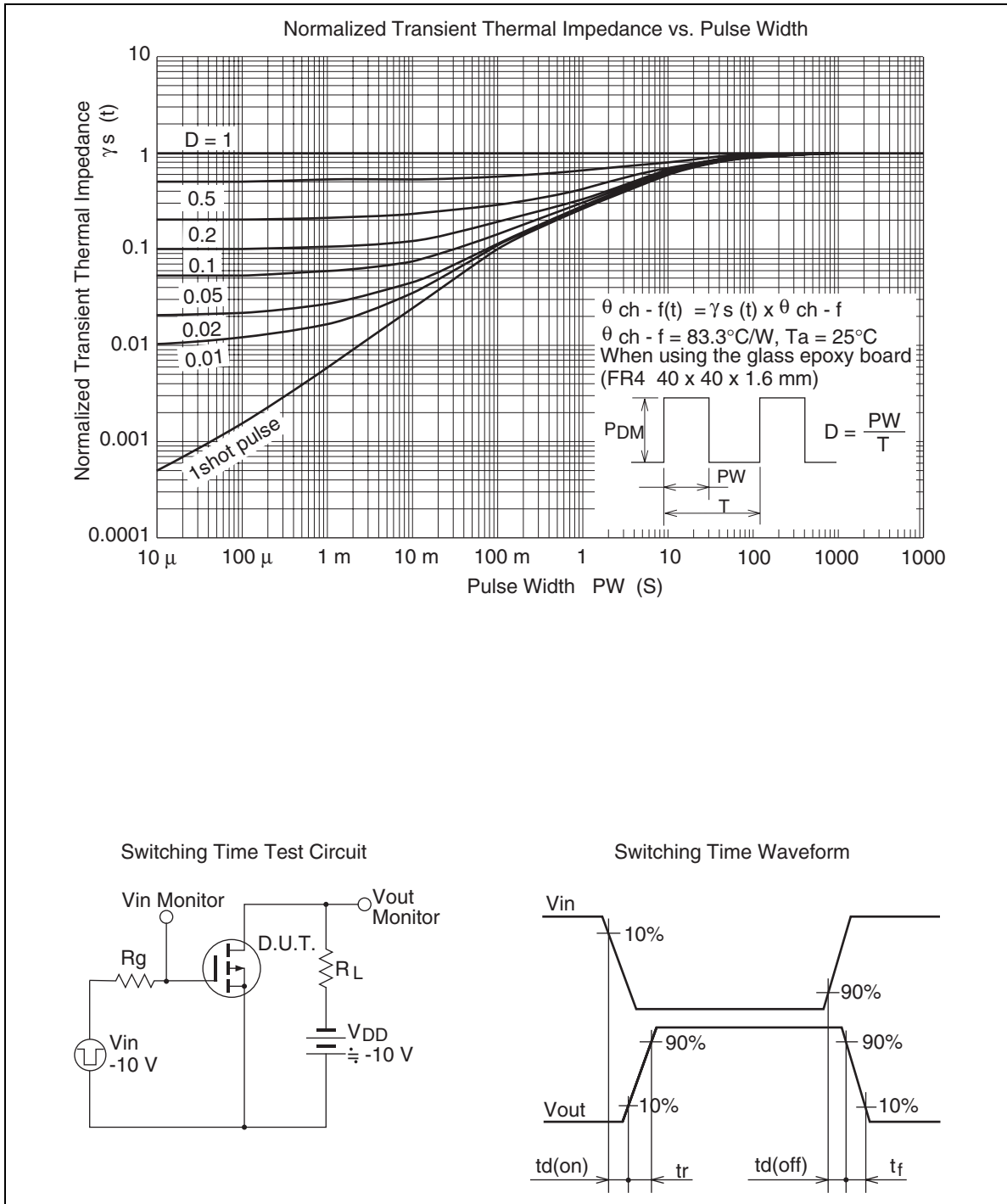


Avalanche Test Circuit



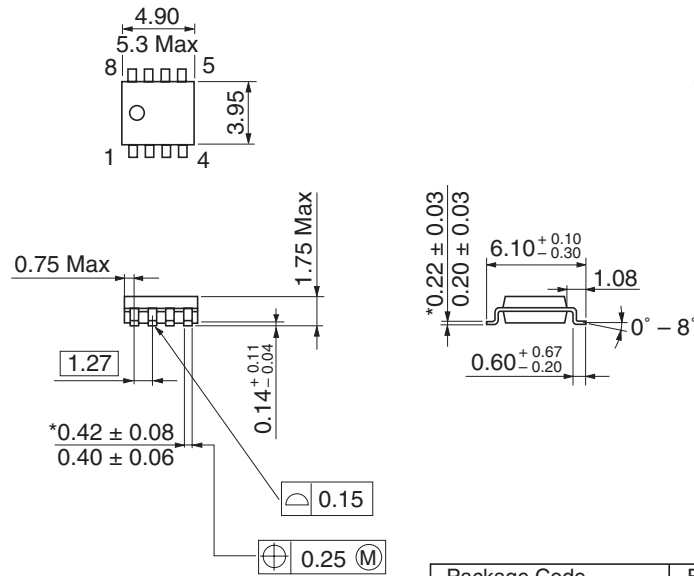
Avalanche Waveform





Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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