High-Speed, Low r_{ON}, SPDT Analog Switch

(2:1 Multiplexer/Demultiplexer Bus Switch)

DESCRIPTION

The DG3157 is a high-speed single-pole double-throw, low power, TTL-Compatible bus switch. Using sub-micro CMOS technology, the DG3157 achieves low on-resistance and negligible propagation delay.

The DG3157 can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} to be transmitted in either direction.

When the Select pin is low, B_0 is connected to the output A pin. When the Select pin is high, B_1 is connected to the output A pin. The path that is open will have a high-impedance state with respect to the output. Make-before-break is guaranteed. An eptiaxial layer prevents latch-up.

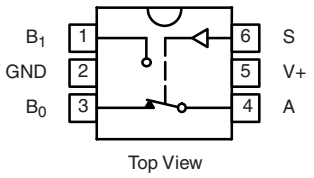
FEATURES

- Direct Cross to Industry Standard *SN74LVC1G3157, NC7SB3157, NLASB3175, PI5A3157, and STG3157*
- SC-70 6-Lead Package
- 1.65 V to 5.5 V V_{CC} Operation
- 5 Ω Connection Between Ports
- Minimal Propagation Delay
- Break-Before-Make Switching
- Zero Bounce In Flow-Through Mode

Pb-free Available

RoHS* COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: G1

TRUTH TABLE	
Logic Input (S)	**Function**
0	B_0 Connected to A
1	B_1 Connected to A

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	SC70-6	DG3157DL-T1 DG3157DL-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
S, A, B[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	D Suffix	- 65 to 150	°C
Power Dissipation (Packages)[b]	6-Pin SC70[c]	250	mW

Notes:
a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_S = 0.25 V to 0.7 V+[e]		Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
DC Characteristics								
High Level Input Voltage	V_{SH}	V+ = 1.65 to 1.95 V		Full	0.75 V+			V
		V+ = 2.3 to 5.5 V		Full	0.7 V+			
Low Level Input Voltage	V_{SL}	V+ = 1.65 to 1.95 V		Full			0.25 V+	
		V+ = 2.3 to 5.5 V		Full			0.3 V+	
On Resistance	R_{ON}	V+ = 4.5 V	V_{BN} = 0 V, I_A = 30 mA	Full		6	7	Ω
			V_{BN} = 2.3 V, I_A = - 30 mA	Full		6	12	
			V_{BN} = 4.5 V, I_A = - 30 mA	Full		9	15	
		V+ = 3.0 V	V_{BN} = 0 V, I_A = 24 mA	Full		8	9	
			V_{BN} = 3.0 V, I_A = - 24 mA	Full		12	20	
		V+ = 2.3 V	V_{BN} = 0 V, I_A = 8 mA	Full		9	12	
			V_{BN} = 2.3 V, I_A = - 8 mA	Full		13	30	
		V+ = 1.65 V	V_{BN} = 0 V, I_A = 4 mA	Full		12	20	
			V_{BN} = 1.8 V, I_A = - 4 mA	Full		18	50	
On Resistance Flatness	R_{FLAT}	0 < V_{BN} < V+	V+ = 4.5 V, I_A = - 30 mA	Room		6		
			V+ = 3.0 V, I_A = - 24 mA	Room		12		
			V+ = 2.3 V, I_A = - 8 mA	Room		22		
			V+ = 1.65 V, I_A = - 4 mA	Room		90		
On Resistance Matching Between Channels	ΔR_{ON}	V+ = 4.5 V, V_{BN} = 3.15 V, I_A = - 30 mA		Room		0.32		
		V+ = 3.0 V, V_{BN} = 2.1 V, I_A = - 24 mA		Room		0.31		
		V+ = 2.3 V, V_{BN} = 1.6 V, I_A = - 8 mA		Room		0.30		
		V+ = 1.65 V, V_{BN} = 1.15 V, I_A = - 4 mA		Room		0.29		
Input Leakage Current	I_S	V+ = 5.5 V, V_A = 5.5 V		Room Full	- 0.1 - 1.0		0.1 - 1.0	µA
Off Stage Switch Leakage	$I_{BN(off)}$	V+ = 5.5 V, V_A/V_B = 0 V/5.5 V		Room Full	- 0.1 - 1.0		0.1 - 1.0	
On State Switch Leakage	$I_{BN(on)}$	V+ = 5.5 V, V_A/V_B = 0 V/5.5 V		Room Full	- 0.1 - 1.0		0.1 - 1.0	
Power Supply								
Power Supply Range	V+			Full	1.65		5.5	V
Quiescent Supply Current	I+	V+ = 5.5 V, V_A = V_B = V+ or GND		Room Full			1 10	µA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_S = 0.25 V to 0.7 V+[e]		Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
AC Electrical Characteristice								
Prop Delay Time[f]	t_{PHL}/t_{PLH}	V_A = 0 V	V+ = 1.65 to 1.95 V	Full				ns
			V+ = 2.3 to 2.7 V	Full		1.2		
			V+ = 3.0 to 3.6 V	Full		0.8		
			V+ = 4.5 to 5.5 V	Full		0.3		
Output Enable Time[f]	t_{PZL}/t_{PZH}	V_{LOAD} = 2 x V+ for t_{PZL} V_{LOAD} = 0 V for t_{PZH}	V+ = 1.65 to 1.95 V	Room Full		10.2 10.4		
			V+ = 2.3 to 2.7 V	Room Full		5.9 6.2		
			V+ = 3.0 to 3.6 V	Room Full		4.1 4.5		
			V+ = 4.5 to 5.5 V	Room Full		2.6 2.9		
Output Disable Time[f]	t_{PLZ}/t_{PHZ}	V_{LOAD} = 2 x V+ for t_{PLZ} V_{LOAD} = 0 V for t_{PHZ}	V+ = 1.65 to 1.95 V	Room Full		10.2 10.4		
			V+ = 2.3 to 2.7 V	Room Full		5.9 6.2		
			V+ = 3.0 to 3.6 V	Room Full		4.1 4.5		
			V+ = 4.5 to 5.5 V	Room Full		2.6 2.9		
Break-Before-Make Time[d]	t_{BBM}	V+ = 1.65 to 1.95 V		Full	0.5			
		V+ = 2.3 to 2.7 V		Full	0.5			
		V+ = 3.0 to 3.65		Full	0.5			
		V+ = 4.5 to 5.5 V		Full	0.5			
Charge Injection[d]	Q	C_L = 0.1 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	V+ = 5 V	Room		7		pC
			V+ = 3.3 V	Room		3		
Analog Switch Characteristics								
Off Isolation[d]	OIRR	R_L = 50 Ω, f = 10 MHz		Room		- 57.6		dB
Crosstalk[d]	X_{TALK}			Room		- 58.7		
- 3-db Bandwidth[d]	BW	R_L = 50 Ω		Room		> 250		MHz
Capacitance								
Control Pin Capacitance[d]	C_{IN}	V+ = 0 V		Room		4.9		pF
B Port Off Capacitance[d]	C_{IO-B}	V+ = 5 V		Room		< 6.5		
A Port Capacitance When Switch Enable[d]	$C_{IO-A(on)}$			Room		< 18.5		

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Typical values are for design aid only, not guaranteed nor subject to production testing.

d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

LOGIC DIAGRAM (POSITIVE LOGIC)

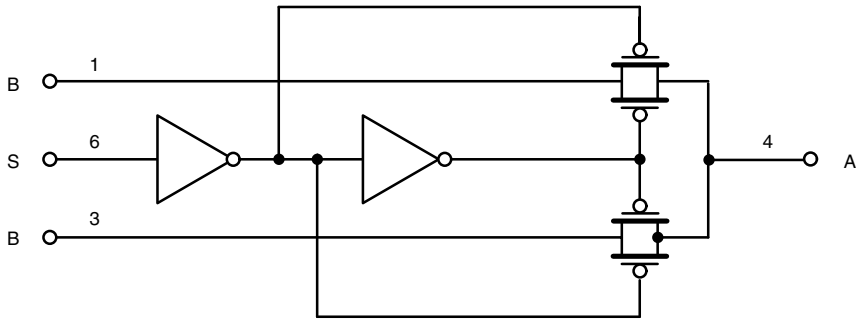
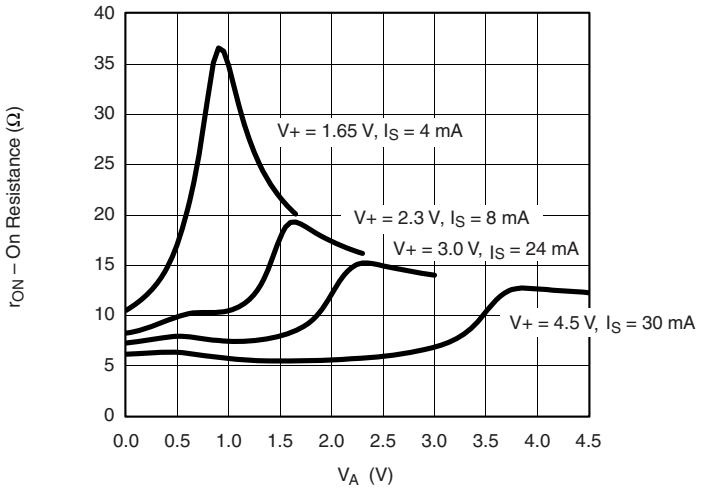


Figure 1.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



r_{ON} vs. V_A vs. V_{CC}

AC LOADING AND WAVEFORMS

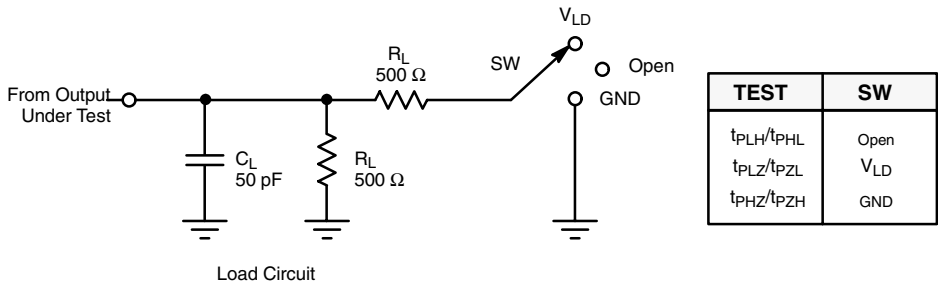


Figure 2. AC Test Circuit

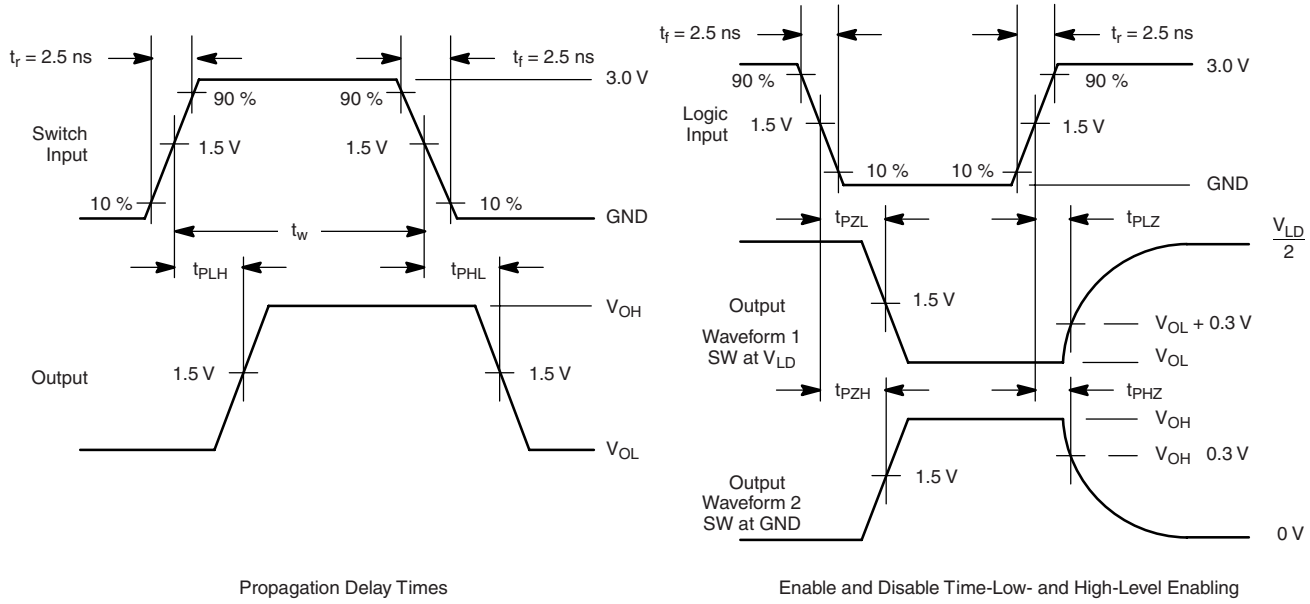
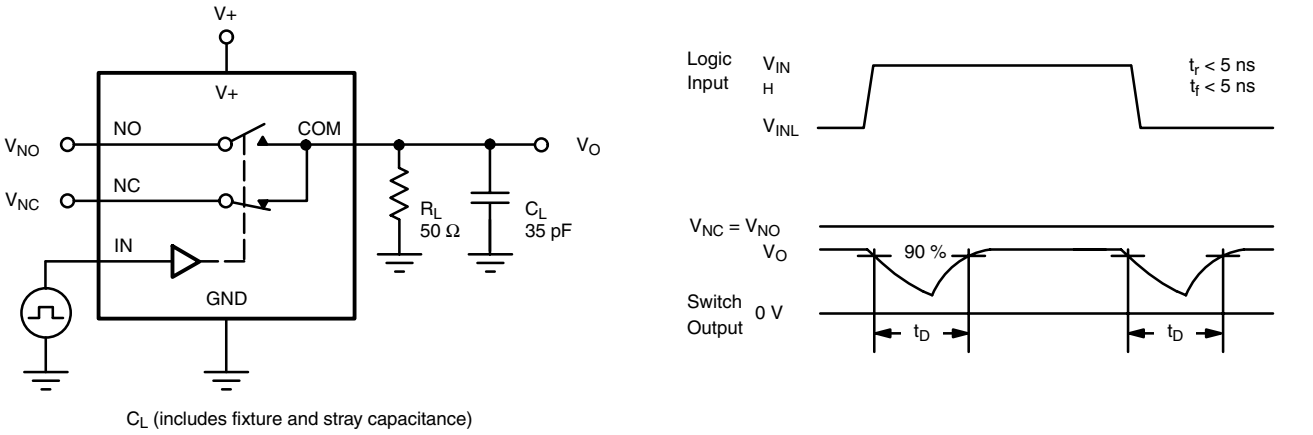


Figure 3. AC Waveforms

Notes:

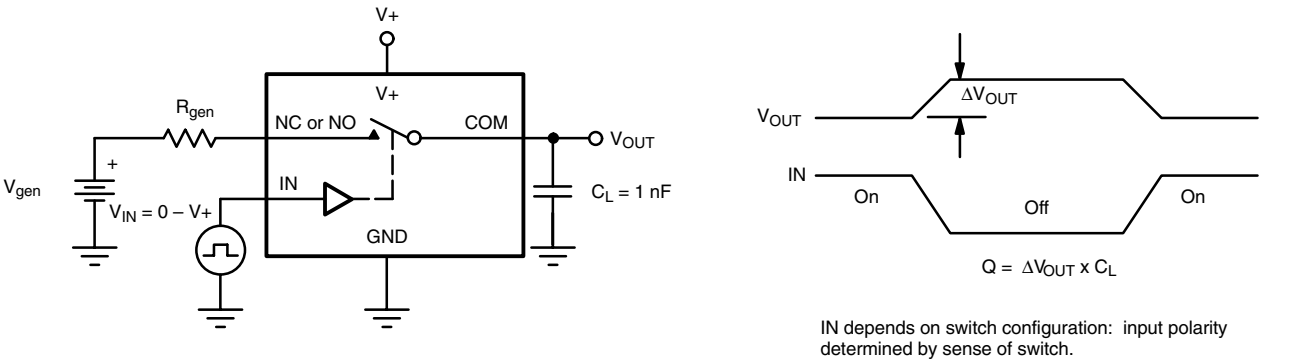
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{dis}.
- t_{PLH} and t_{PHL} are the same as t_{dis}.
- V_{LD} = 2 V+.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 4. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 5. Charge Injection

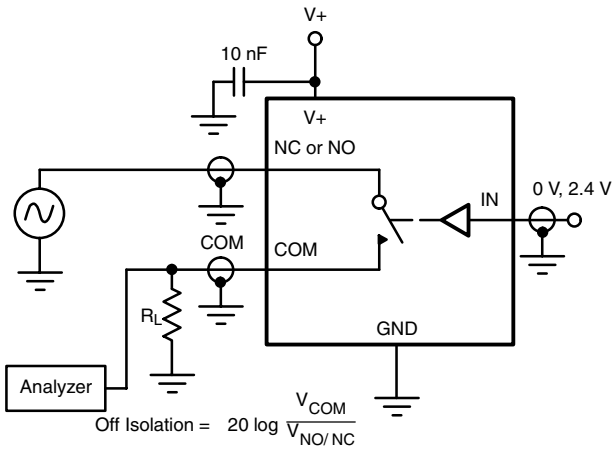


Figure 6. Off-Isolation

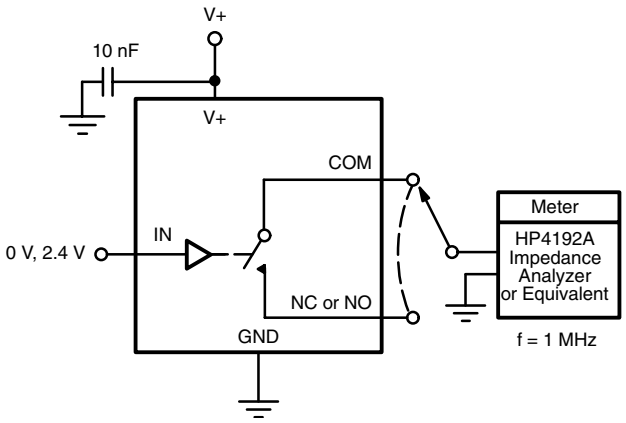


Figure 7. Channel Off/On Capacitance

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