Bi-Directional N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{S1S2} (V)	$r_{S1S2(on)}$ (Ω)	I_{S1S2} (A)
20	0.045 @ V_{GS} = 4.5 V	5.0
	0.048 @ V_{GS} = 3.7 V	4.8
	0.057 @ V_{GS} = 2.5 V	4.4
	0.072 @ V_{GS} = 1.8 V	3.9

FEATURES

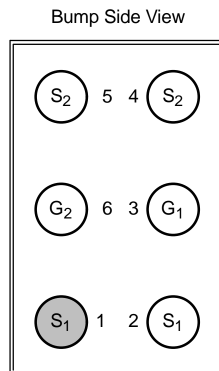
- TrenchFET® Power MOSFET
- Ultra-Low $r_{SS(on)}$
- ESD Protected: 4000 V
- New MICRO FOOT™ Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area

APPLICATIONS

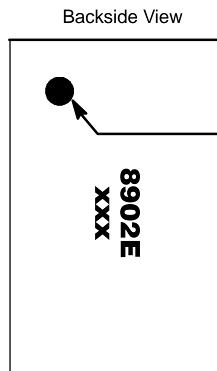
- Battery Protection Circuit
  - 1-2 Cell Li+/LiP Battery Pack for Portable Devices

MICRO FOOT™

Bump Side View



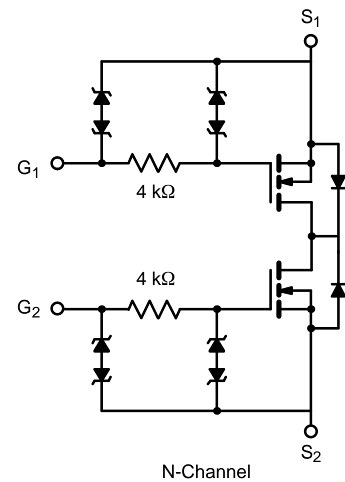
Backside View



Pin 1 Identifier

Device Marking:

8902E = P/N Code
xxx = Date/Lot Traceability Code



N-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Source1—Source2 Voltage		V_{S1S2}	20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Source1—Source2 Current (T_J = 150°C)[a]	T_A = 25°C	I_{S1S2}	5.0	3.9	A
	T_A = 85°C		3.4	2.8	
Pulsed Source1—Source2 Current		I_{SM}	8		
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.7	1	W
	T_A = 85°C		0.8	0.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Package Reflow Conditions[c]	VPR		215		
	IR/Convection		220		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	60	75	°C/W
	Steady State		95	120	
Maximum Junction-to-Foot[b]	Steady State	R_{thJF}	18	22	

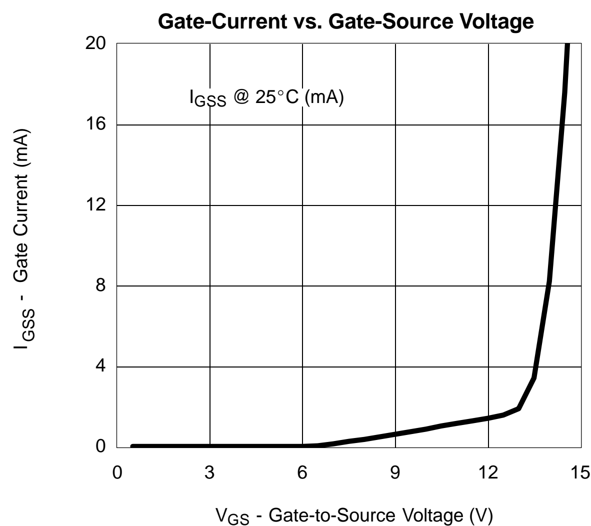
Notes
a. Surface Mounted on 1” x 1” FR4 Board.
b. The Foot is defined as the top surface of the package.
c. Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.

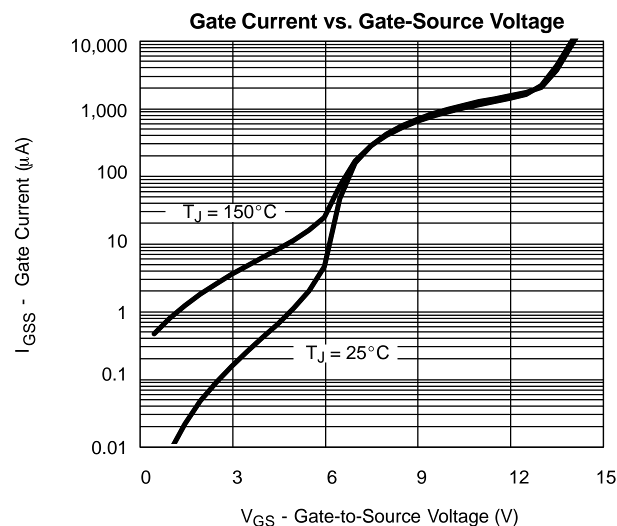
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{SS} = V_{GS}$, I_D = 980 µA	0.45		1.0	V
Gate-Body Leakage	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±4.5 V			±4	µA
		V_{SS} = 0 V, V_{GS} = ±12 V			±10	mA
Zero Gate Voltage Source Current	I_{S1S2}	V_{SS} = 16 V, V_{GS} = 0 V			1	µA
		V_{SS} = 16 V, V_{GS} = 0 V, T_J = 85°C			5	
On-State Source Current[a]	$I_{S(on)}$	V_{SS} = 5 V, V_{GS} = 4.5 V	5			A
Source1—Source2 On-State Resistance[a]	$r_{S1S2(on)}$	V_{GS} = 4.5 V, I_{SS} = 1 A		0.038	0.045	Ω
		V_{GS} = 3.7 V, I_{SS} = 1 A		0.041	0.048	
		V_{GS} = 2.5 V, I_{SS} = 1 A		0.048	0.057	
		V_{GS} = 1.8 V, I_{SS} = 1 A		0.060	0.072	
Forward Transconductance[a]	g_{fs}	V_{SS} = 10 V, I_{SS} = 1 A		20		S
Dynamic[b]						
Turn-On Delay Time	$t_{d(on)}$	V_{SS} = 10 V, R_L = 10 Ω I_{SS} ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		1	1.5	µs
Rise Time	t_r			3	4.5	
Turn-Off Delay Time	$t_{d(off)}$			17	26	
Fall Time	t_f			10	15	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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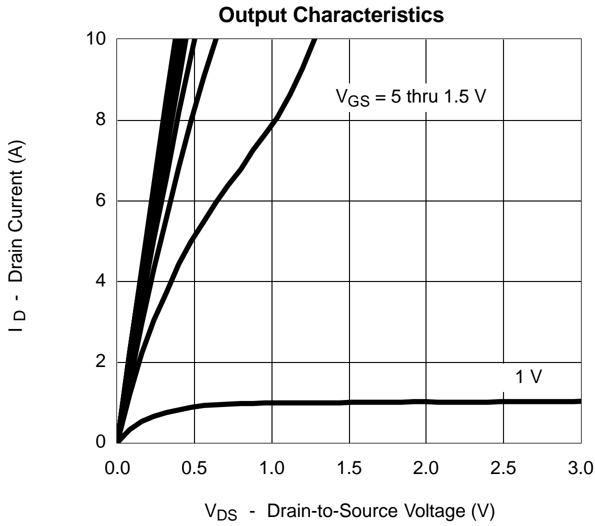
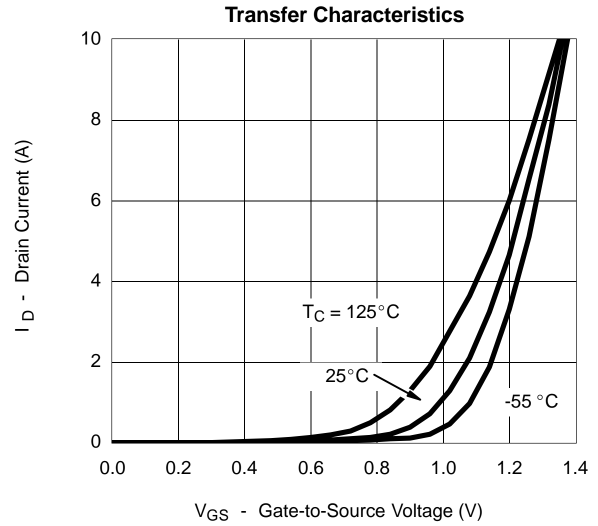
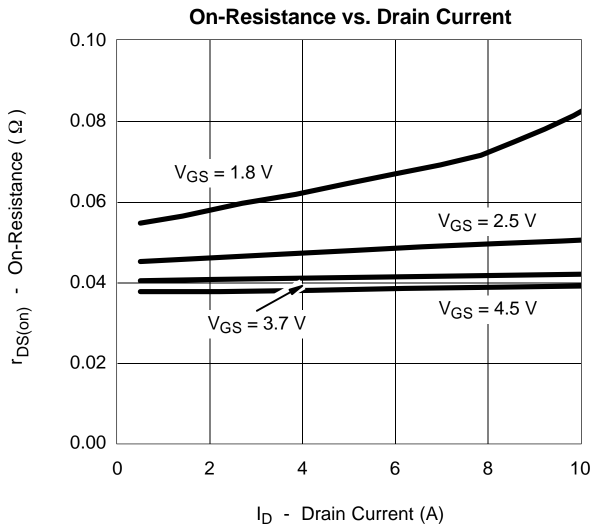
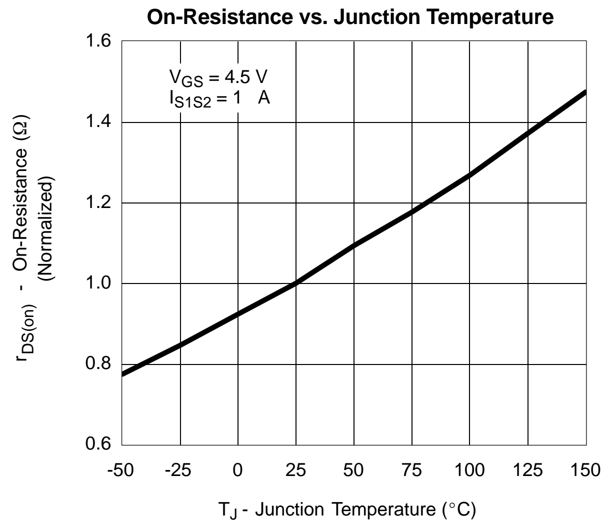
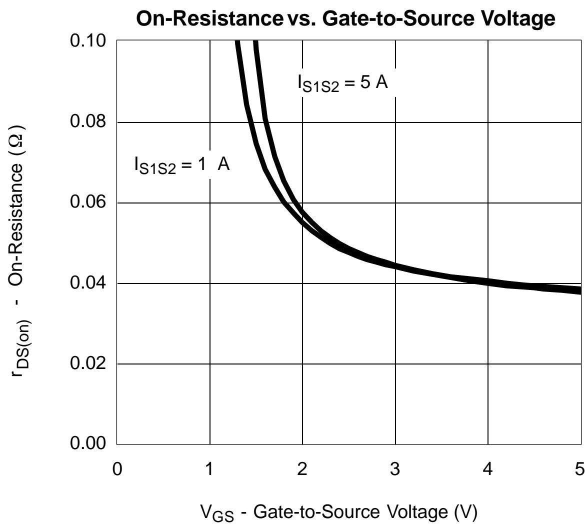
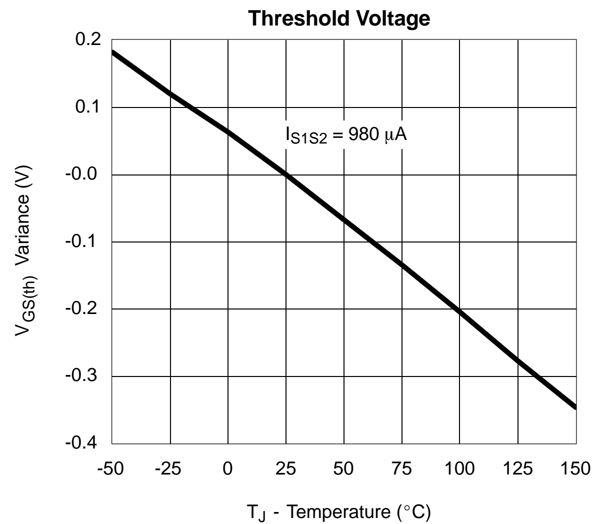






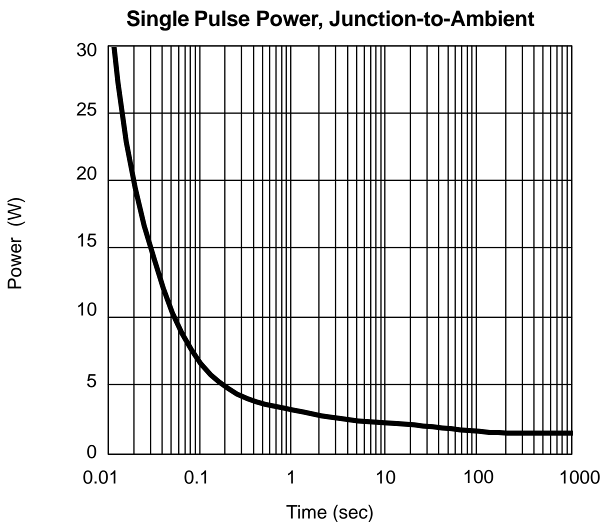




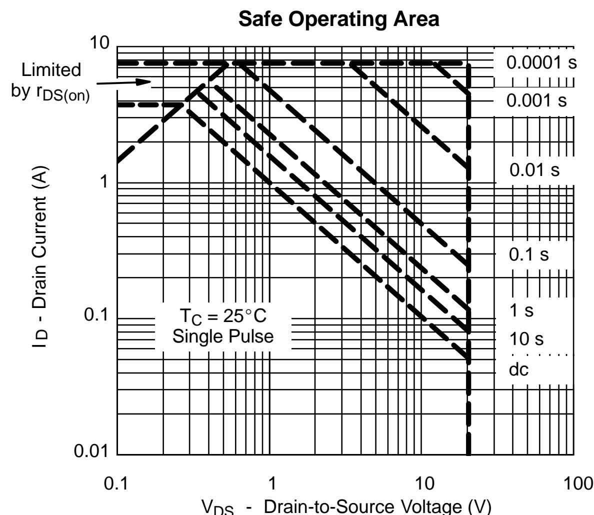


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

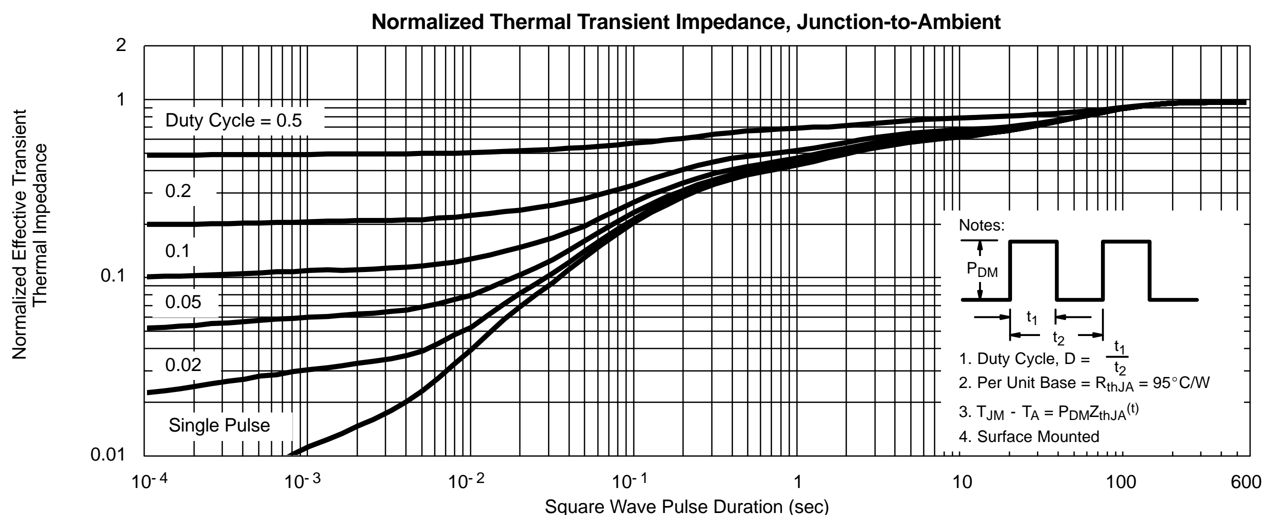
Single Pulse Power, Junction-to-Ambient



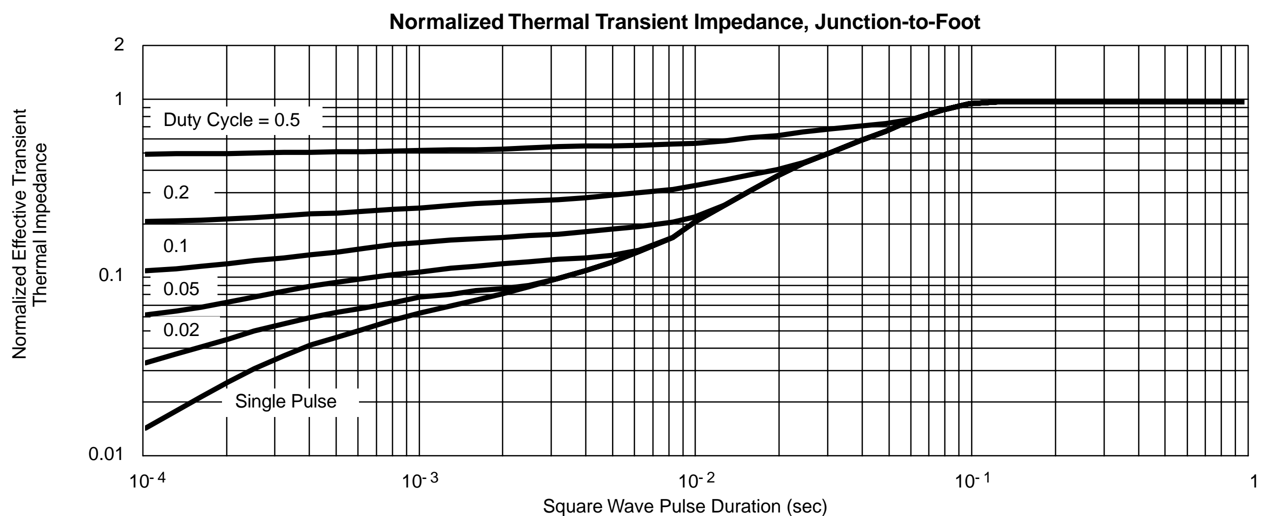
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

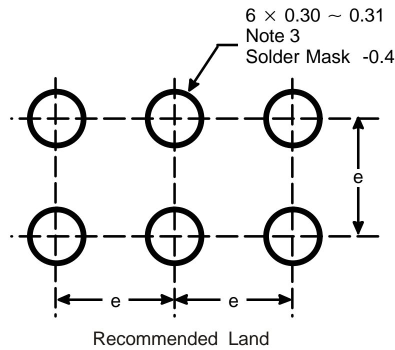


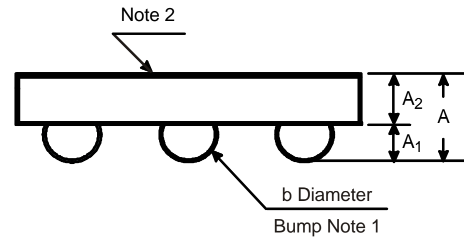
Normalized Thermal Transient Impedance, Junction-to-Foot

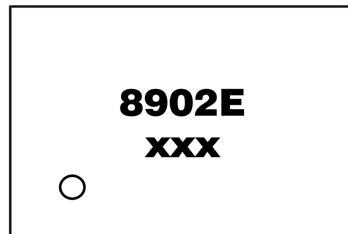


PACKAGE OUTLINE

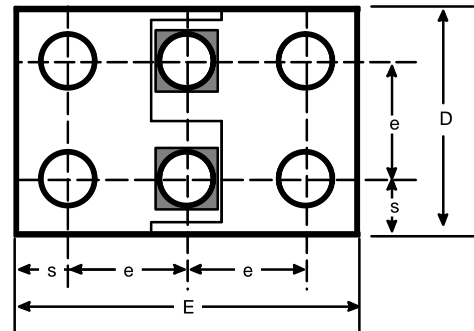
MICRO FOOT: 6-BUMP (2 X 3, 0.8-mm PITCH)







Mark on Backside of Die



NOTES (Unless Otherwise Specified):

1. 6 solder bumps are Eutetic 63Sn/37Pb with diameter 0.37 - 0.41 mm
2. Backside surface is coated with a Ag/Ni/Ti layer
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.102	0.114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

* Use millimeters as the primary measurement.