ESDALC6V1W5

QUAD TRANSIL™ ARRAY FOR ESD PROTECTION

Application Specific Discretes
A.S.D.

MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment
- Set top boxes

FEATURES

- 4 unidirectional TRANSIL™ functions.
- ESD Protection: IEC61000-4-2 level 4
- Breakdown voltage V_{BR} = 6.1V min
- Low leakage current < 1µA @ 3 Volts
- Low capacitance device

DESCRIPTION

The ESDALC6V1W5 is a 4-bit wide monolithic suppressor which is designed to protect component connected to data and transmission lines against ESD.

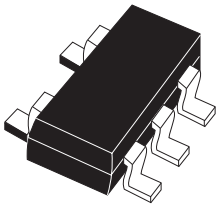
It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

BENEFITS

- High ESD protection level : up to 25 kV.
- Capacitance: 12pF @ 0V Typ.
- High integration.
- Suitable for high density boards.

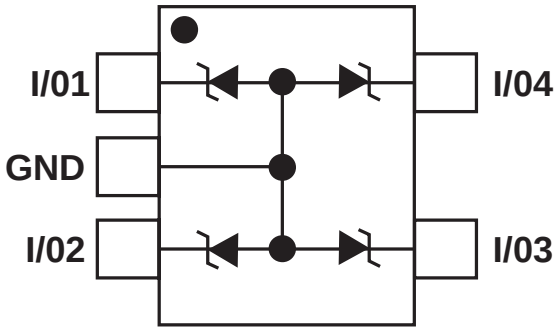
COMPLIES WITH THE FOLLOWING STANDARDS :

- IEC61000-4-2 level 4: 15 kV (air discharge)
  8 kV (contact discharge)
- MIL STD 883C-Method 3015-6 : class 3.
  (human body model) 25kV (HBM)



SOT323-5L

FUNCTIONAL DIAGRAM

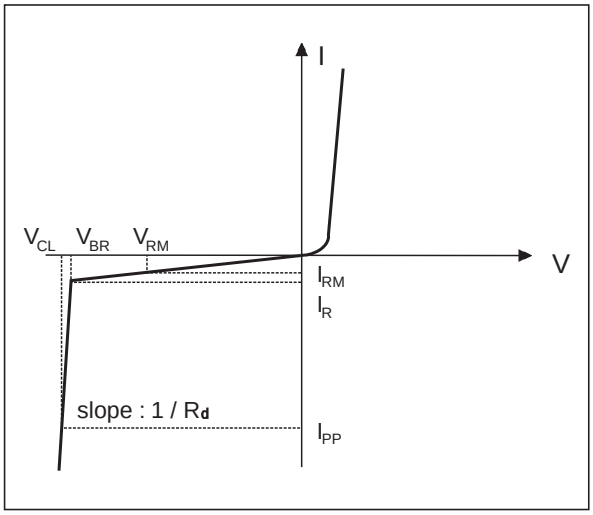


ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP}	ESD discharge - MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		± 25 ± 15 ± 8	kV
P_{PP}	Peak pulse power (8/20 µs)		25	W
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_{op}	Operating temperature range		- 40 to + 150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
C	Capacitance per line
Rd	Dynamic resistance



Types	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C	C
	min.	max.		max.		typ. note 1	max. note 2	typ. 3V bias	max. 3V bias
	V	V	mA	µA	V	mΩ	10^{-4}/°C	pF	pF
ESDALC6V1W5	6.1	7.2	1	1	3	1100	6	7.5	9.5

Note 1 : Square pulse Ipp = 15A, tp=2.5µs.
Note 2 : $\Delta V_{BR} = \alpha T^* (Tamb - 25°C) * V_{BR}$ (25°C)

Fig. 1: Relative variation of peak pulse power versus initial junction temperature.

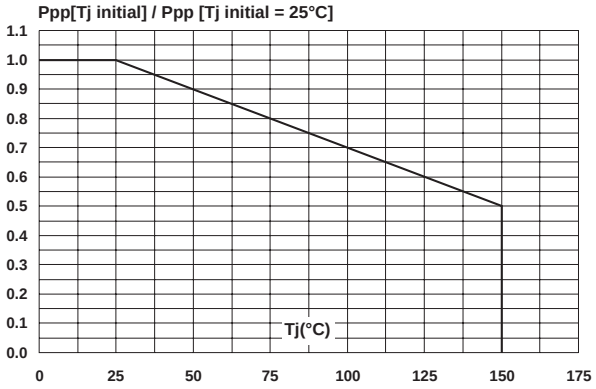


Fig. 2: Peak pulse power versus exponential pulse duration.

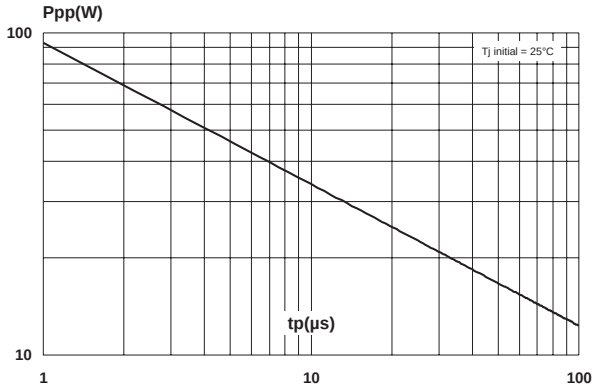


Fig. 3: Junction capacitance versus reverse voltage applied (typical values).

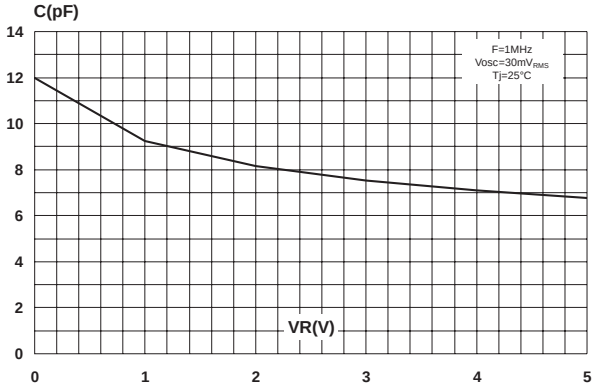


Fig. 4: Clamping voltage versus peak pulse current (maximum values, rectangular waveform).

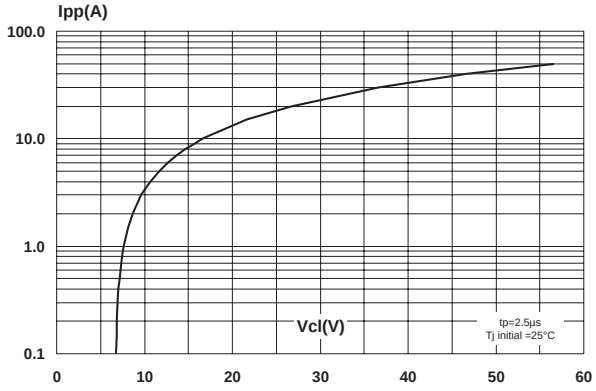


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).

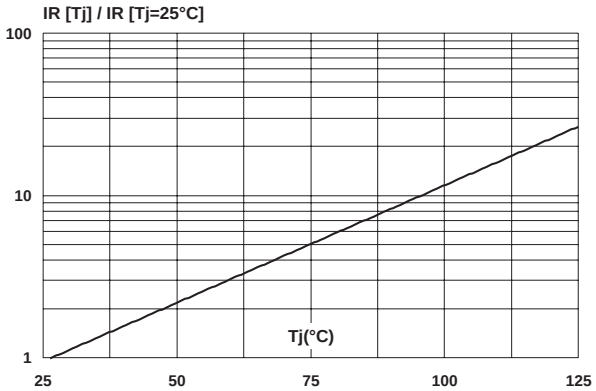
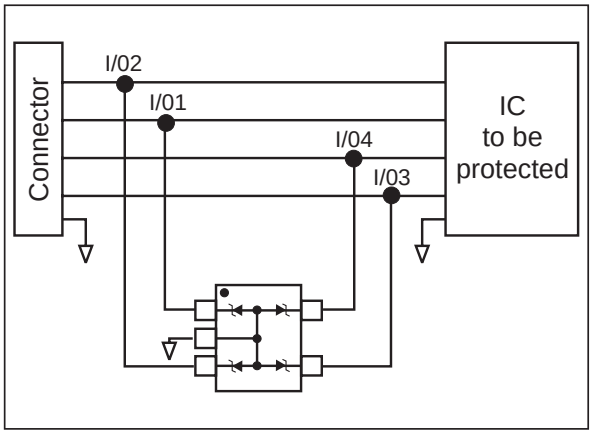


Fig. 6: Application example



TECHNICAL INFORMATION

1. ESD protection by ESDALC6V1W5

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

As a transient voltage suppressor, ESDALC6V1W5 is an ideal choice for ESD protection by suppressing ESD events. It is capable of clamping the incoming transient to a low enough level such that any damage is prevented on the device protected by ESDALC6V1W5.

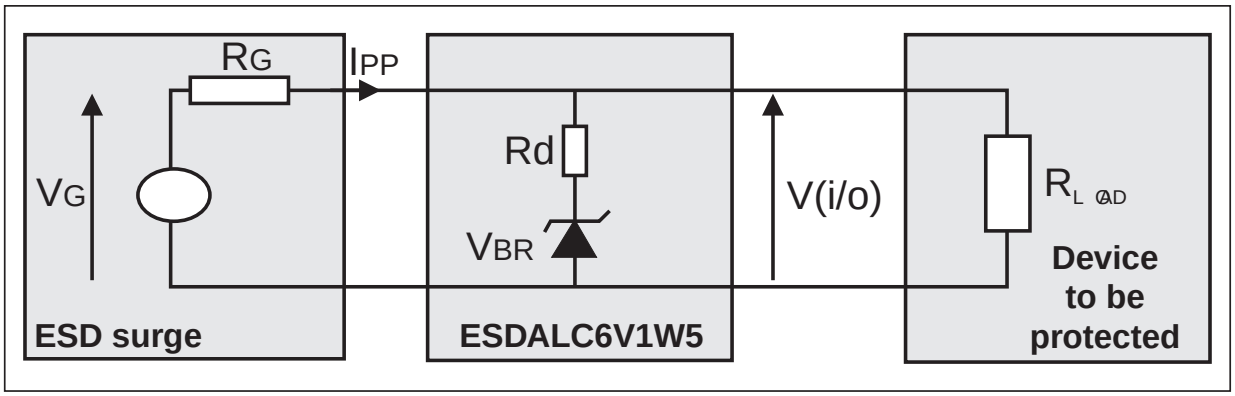
ESDALC6V1W5 serves as a parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the ESDALC6V1W5 becomes a low impedance path diverting the transient current to ground.

The clamping voltage is given by the following formula:

$$V_{CL} = V_{BR} + Rd.I_{PP}$$

As shown in figure A1, the ESD strikes are clamped by the transient voltage suppressor.

Fig. A1: ESD clamping behavior



To have a good approximation of the remaining voltages at both Vi/o side, we provide the typical dynamical resistance value Rd. By taking into account the following hypothesis:

$$Rg > Rd \text{ and } Rload > Rd$$

we have:

$$V(i/o) = V_{BR} + R_d \times \frac{V_g}{R_g}$$

The results of the calculation done Vg = 8kV, Rg = 330Ω (IEC61000-4-2 standard), V_{BR} = 6.1V (min) and Rd = 1.1Ω (typ.) give:

$$V(i/o) = 32{,}8 Volts$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the Vi/o side.

Fig. A2: ESD test board

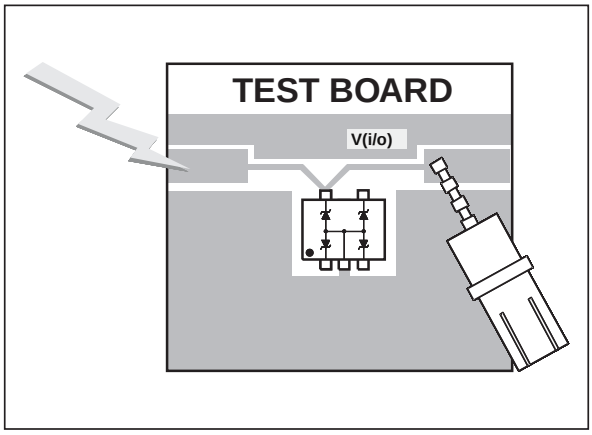
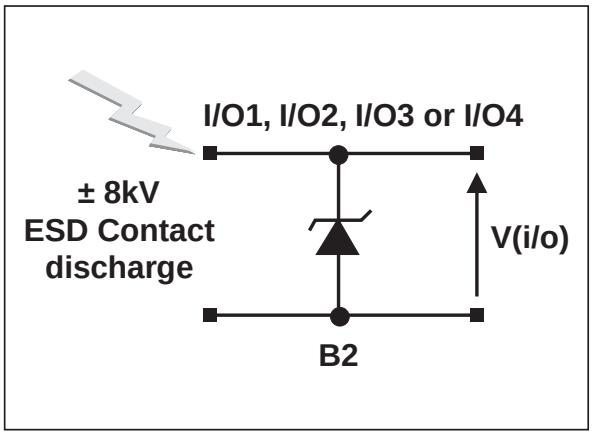
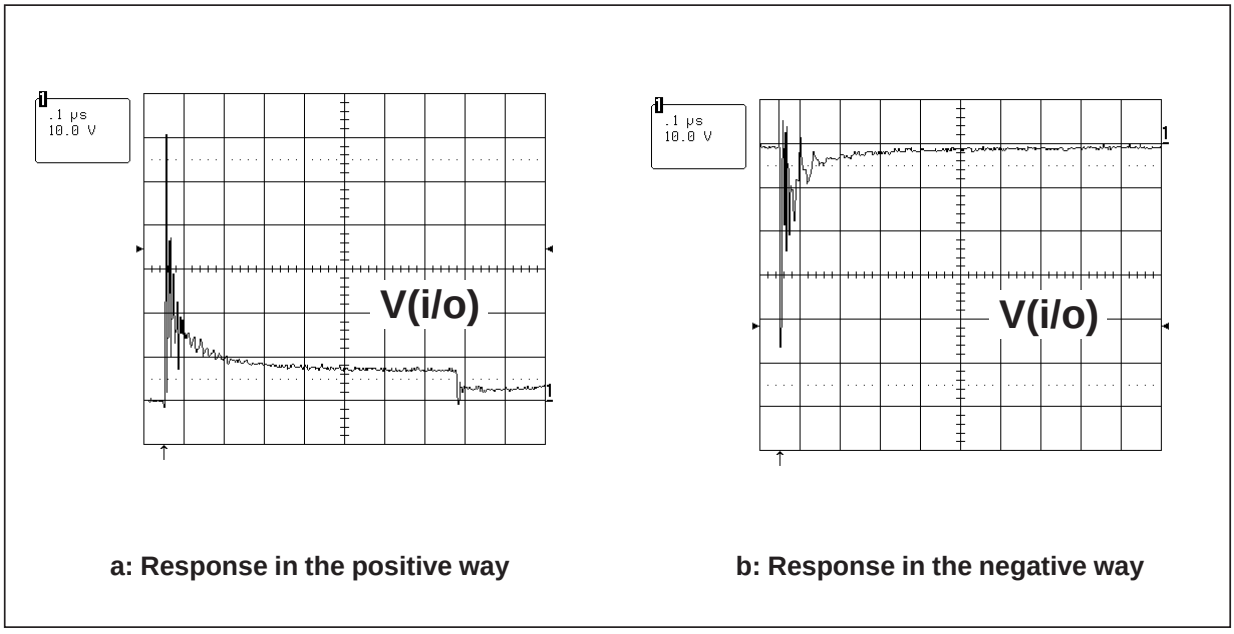


Fig. A3: ESD test configuration



The measurements done here after show very clearly (Fig. A4) the high efficiency of the ESD protection: the clamping voltage V(i/o) becomes very close to $+V_{BR}$ (positive way, Fig. A4a) and $-V_{BR}$ (negative way, Fig. A4b).

Fig. A4: Remaining voltage during ESD surge

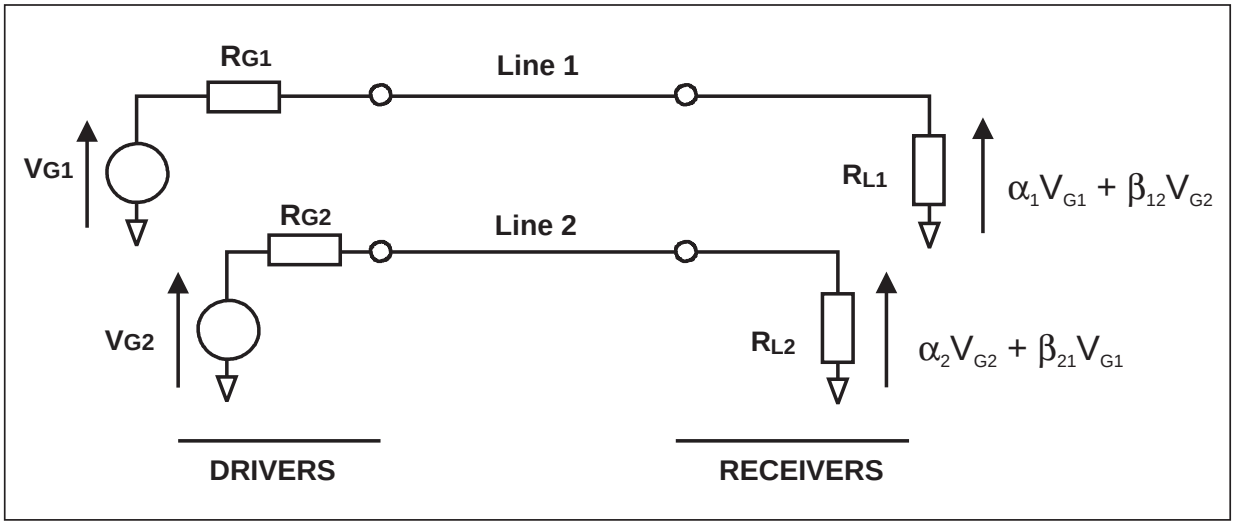


a: Response in the positive way

b: Response in the negative way

CROSSTALK BEHAVIOR

Fig. A5: Crosstalk phenomenon



The crosstalk phenomena are due to the coupling between 2 lines. Coupling factors ($\beta 12$ or $\beta 21$) increase when the gap across lines decreases, particularly in silicon dice. In the example above, the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G2}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ)

Fig. A6: Analog crosstalk measurements

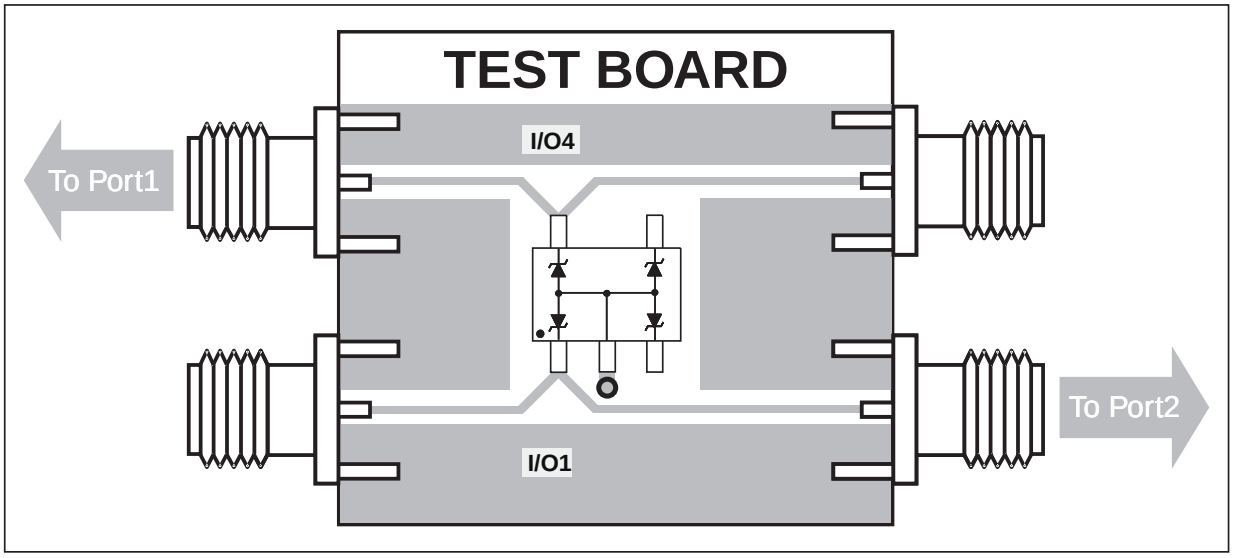


Fig. A7: Typical analog crosstalk measurements.

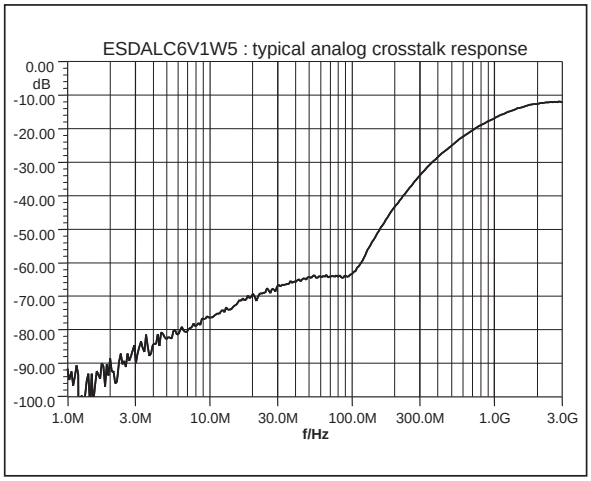


Figure A6 gives the measurement circuit for the analog crosstalk application. In figure A7, the curve shows the effect of the line I/O1 on the line I/O4. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -60dB.

Fig. A8: Digital crosstalk measurements configuration.

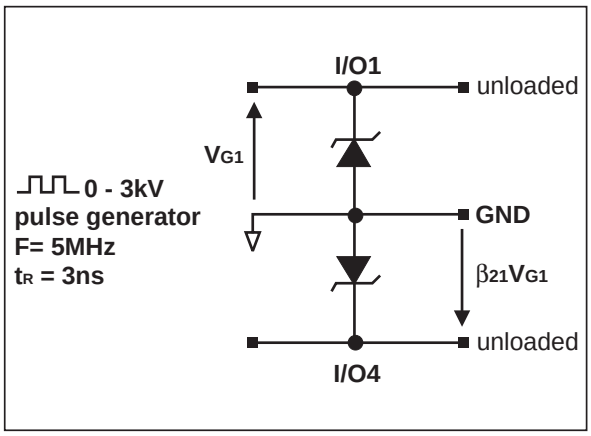


Fig. A9: Digital crosstalk results.

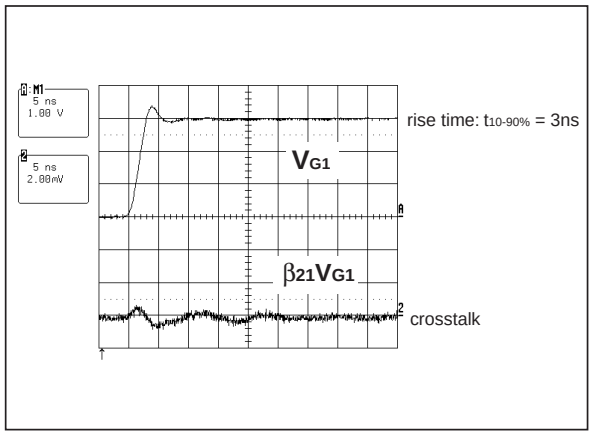
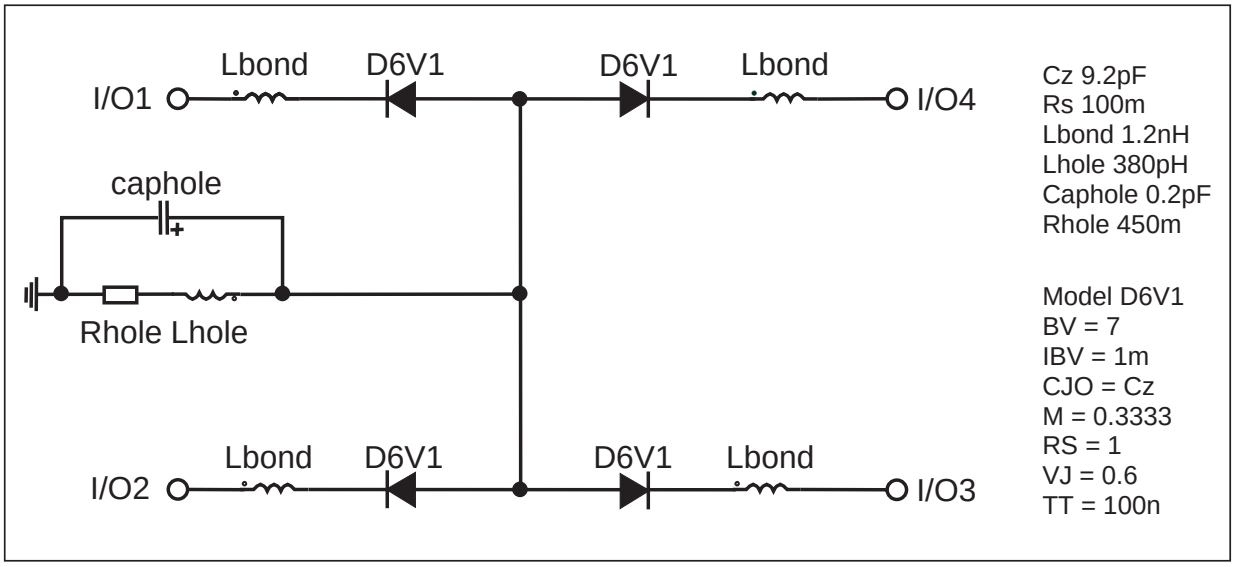
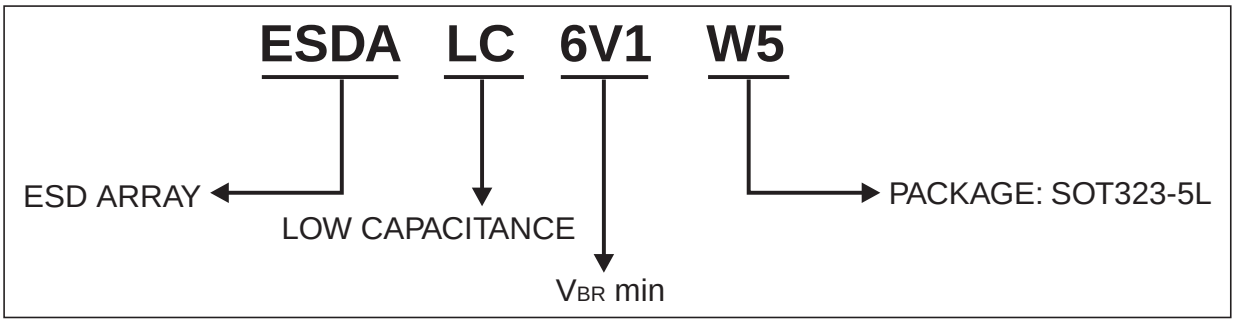


Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.
Figure A9 shows that in such a condition, the impact on the disturbed line is less than 50 mV peak to peak. No data disturbance was noted on the concerned line. The measurements performed with falling edges give an impact within the same range.

Fig. A10: Aplac model



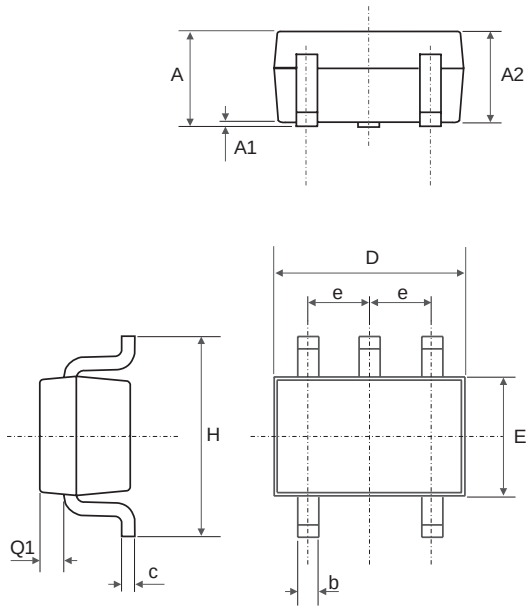
ORDER CODE



Ordering type	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1W5	C61	SOT323-5L	5.4 mg.	3000	Tape & reel

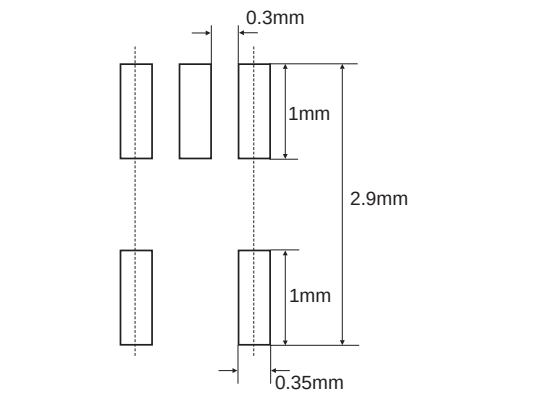
PACKAGE MECHANICAL DATA

SOT323-5L



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.026 Typ.	
H	1.8	2.4	0.071	0.094
Q1	0.1	0.4	0.004	0.016

FOOT PRINT (in millimeters)



Mechanical specifications	
Lead plating	Tin-lead
Lead plating thickness	5µm min. 25 µm max.
Lead material	Sn / Pb (70% to 90% Sn)
Lead coplanarity	10µm max.
Body material	Molded epoxy
Epoxy meets	UL94,V0