TOSHIBA MULTI CHIP DISCRETE DEVICE

HN2E01F

Super High Speed Switching Application Audio Frequency Amplifier Application General Switching Application

Q1

Q2

 $\begin{array}{lll} \mbox{High DC Current Gain} & : & \mbox{h}_{\mbox{FE}} = 600 \sim 3600 \\ \mbox{High Voltage} & : & \mbox{V}_{\mbox{CEO}} = 50 \mbox{V} \\ \mbox{High Collector Current} & : & \mbox{I}_{\mbox{C}} = 150 \mbox{mA}(\mbox{max.}) \end{array}$

Q1 (Diode) : 1SS352 Equivalent
Q2 (Transistor) : 2SC4666 Equivalent

Q1 (Diode) Absolute Maximum Ratings (Ta = 25°C)

| Characteristic | Symbol | Rating | Unit |
|--------------------------------|-------------------|--------|----------|
| Maximum (peak) reverse voltage | V _{RM} (| 85 | y |
| Reverse voltage | VR | 80 | <u> </u> |
| Maximum (peak) forward current | I _{FM} | 300 | mA |
| Average forward current | P | 100 | _ mA |
| Surge current (10ms) | (FSM) | 1 | A |

Unit: mm 2.8-0.3 1.6-0.1 1.6-0.1 1.Anode 2.Base 3.Collector 4.Emitter 5.NC 6.Cathode JEDEC JETA TOSHIBA 2-3N1D

Weight: 0.015g (typ.)

Q2 (Transistor) Absolute Maximum Ratings (Ta = 25°C)

| Characteristic | Symbol | Rating | Unit |
|---------------------------|--------------------|--------|------|
| Collector-base voltage | → V _{CBO} | 50 | ٧ |
| Collector-emitter voltage | VCEO | 50 | ٧ |
| Emitter-base voltage | V _{EBO} | 5 | V |
| Collector current | ΙÇ | 150 | mA |
| Base current | l _B | 30 | mA |

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

| Characteristic | Symbol | Rating | Unit |
|-----------------------------|------------------|------------|------|
| Collector power dissipation | Pc* | 300 | mW |
| Junction temperature | Тј | 125 | °C |
| Storage temperature range | T _{stg} | -55 to 125 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

^{*} Total rating: 200mW per element should not be exceeded.

Q1 (Diode) Electrical Characteristics (Ta = 25°C)

| Characteristic | Symbol | Test Circuit | Test Condition | Min | Тур. | Max | Unit |
|-----------------------|--------------------|-----------------|-------------------------------|-----|------|-----|------|
| Forward voltage | V _{F (1)} | _ | I _F = 1mA | _ | 0.62 | ı | ٧ |
| | V _{F (2)} | _ | I _F = 10mA | - | 0.75 | 1 | |
| | V _{F (3)} | _ | I _F = 100mA | _ | 0.98 | 1.2 | |
| Reverse current — | I _{R (1)} | _ | V _R = 30V | 1 | _ | 0.1 | μА |
| | I _{R (2)} | _ | V _R = 80V | | /2 | 0.5 | |
| Total capacitance | CT | _ | V _R = 0, f = 1MHz | | 0.5 | 1 | pF |
| Reverse recovery time | t _{rr} | _ | I _F = 10mA (fig.1) | / | 1.6 | _ | ns |

Q2 (Transistor) Electrical Characteristics (Ta = 25°C)

| Characteristic | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------------|----------------------|-----------------|--|------------------------------|------|------|------|
| Collector cut-off current | I _{CBO} | _ | V _{CB} = 50V, t _E = 0 | - 12 | | 100 | nA |
| Emitter cut-off current | I _{EBO} | _ | V _{EB} = 5V, J _C = 0 | +(|)) | 100 | nA |
| DC current gain | h _{FE} * | _ | V _{CE} = 6V, I _C = 2mA | 600 | (1) | 3600 | |
| Collector-emitter saturation voltage | V _{CE(sat)} | _ | IC=100mA, IB=10mA | | 0.12 | 0.25 | V |
| Transition frequency | f _T | < | V _{CE} = 10V, I _C =10mA | $\left(\rightarrow \right)$ | 250 | _ | MHz |
| Collector output capacitance | C _{ob} | | V _{CB} = 10V, I _E = 0,f=1MHz | <u> </u> | 3.5 | | pF |

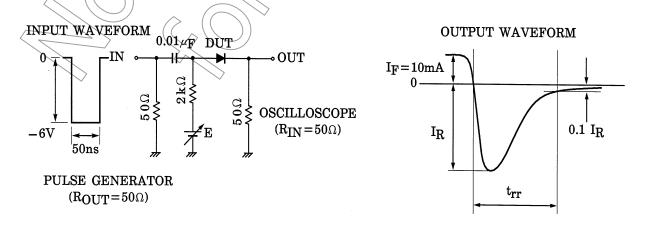
h_{FE} Rank A: 600 to 1800, B: 1200 to 3600

Marking

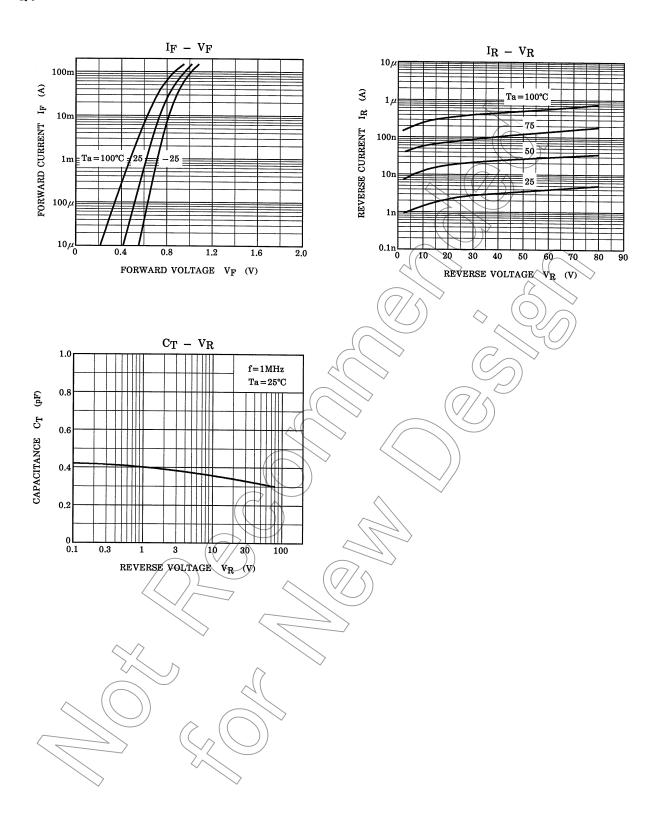
Equivalent Circuit (Top View)



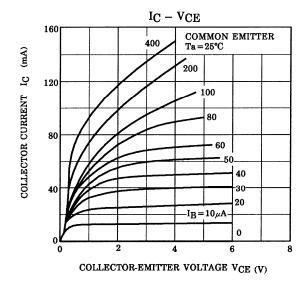
Fig. 1 : Reverse Recovery Time (t_{rr}) Test Circuit

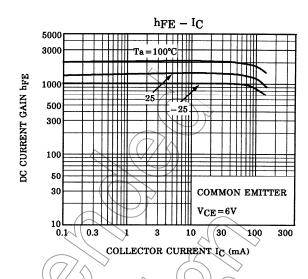


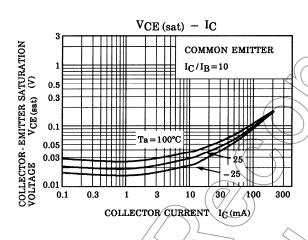
Q1

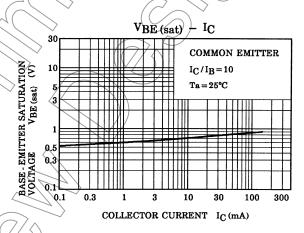


Q2

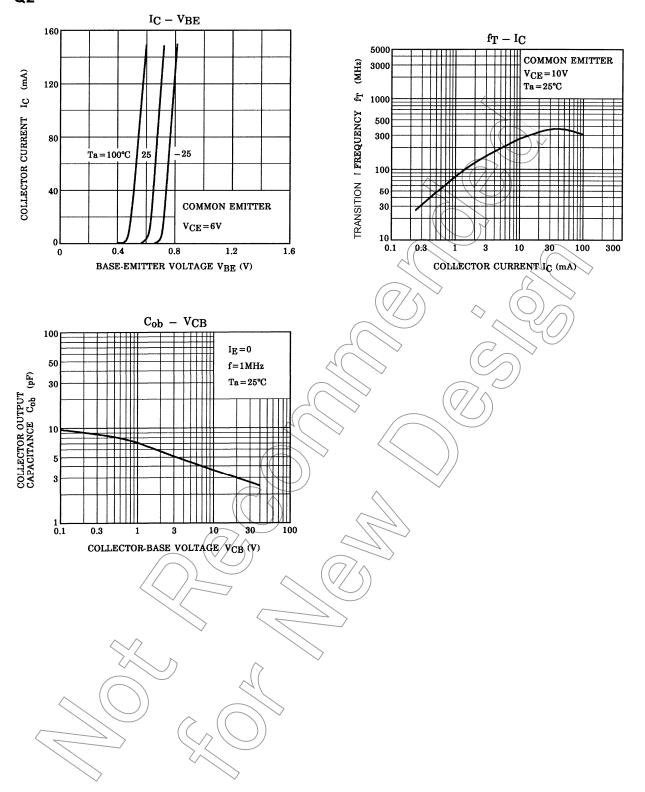






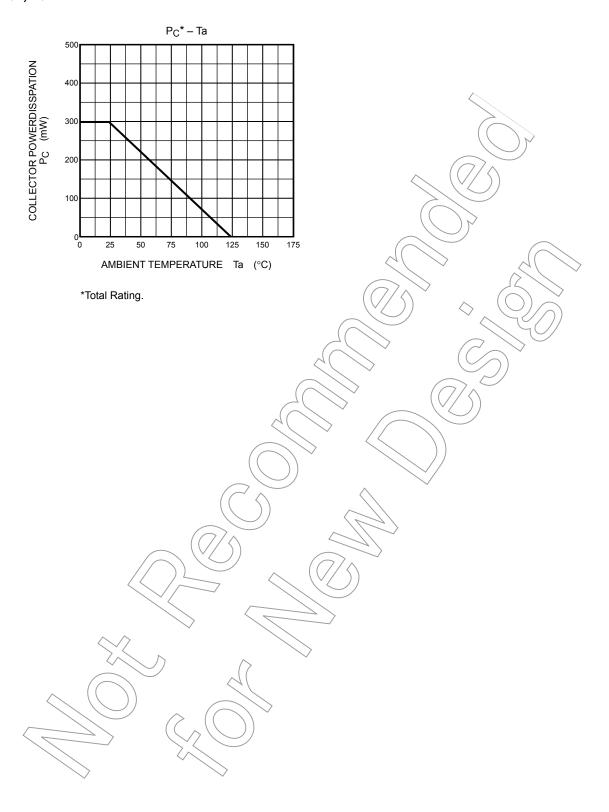


Q2



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Q1, Q2 Common



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