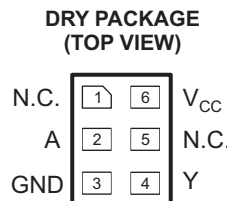# SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT
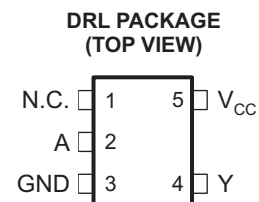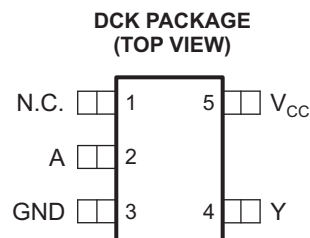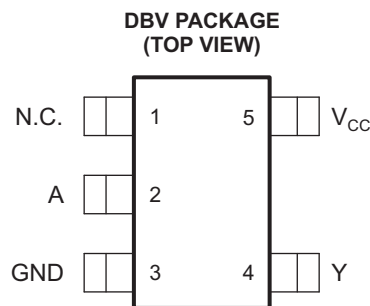
Check for Samples: SN74LVC1G07

FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Supports 5-V V_{CC} Operation**
- **Input and Open-Drain Output Accept Voltages up to 5.5 V**
- **Max t_{pd} of 4.2 ns at 3.3 V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBV PACKAGE
(TOP VIEW)

DCK PACKAGE
(TOP VIEW)

DRL PACKAGE
(TOP VIEW)
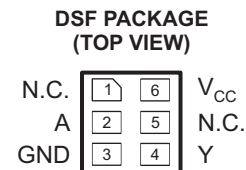
N.C. – No internal connection
See mechanical drawings for dimensions.

DRY PACKAGE
(TOP VIEW)

DSF PACKAGE
(TOP VIEW)

YZP PACKAGE
(TOP VIEW)

DNU – Do not use

YZV PACKAGE
(TOP VIEW)
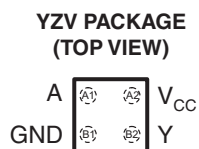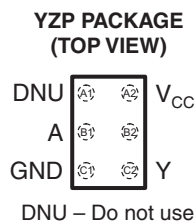
Table 1. YZP PACKAGE TERMINAL ASSIGNMENTS

	1	2
A	DNU	V_{CC}
B	A	No ball
C	GND	Y

Table 2. YZV PACKAGE TERMINAL ASSIGNMENTS

	1	2
A	A	V_{CC}
B	GND	Y

DESCRIPTION/ORDERING INFORMATION

This single buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE[1] [2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G07YZPR	_ _ _CV_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZV (Pb-free)	Reel of 3000	SN74LVC1G07YZVR	− − − − CV
	QFN – DRY	Reel of 5000	SN74LVC1G07DRYR	CV
			SN74LVC1G07DRYRG4	
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G07DBVR	C07_
		Reel of 250	SN74LVC1G07DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G07DCKR	CV_
		Reel of 250	SN74LVC1G07DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G07DRLR	CV_
	µQFN – DSF	Reel	SN74LVC1G07DSFR	CV

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DBV/DCK/DRL/DRY/DSF: The actual top-side marking has one additional character that designates the assembly/test site.
     YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
     YZV: The actual top-side marking is on two lines. Line 1 has four characters to denote year, month, day, and assembly/test site. Line 2 has two characters which show the family and function code. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Table 3. FUNCTION TABLE

INPUT A	OUTPUT Y
L	L
H	Z

LOGIC DIAGRAM (POSITIVE LOGIC)
(DBV, DCK, DRL, DSF, DRY, and YZP Package)

A 2 ▷ 4 Y

LOGIC DIAGRAM (POSITIVE LOGIC)
(YZV Package)

A 1 ▷ 3 Y

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]		−0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DBV package		206	°C/W
		DCK package		252	
		DRL package		142	
		DRY package		234	
		DSF package		300	
		YZP package		132	
		YZV package		116	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC1G07

RECOMMENDED OPERATING CONDITIONS[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ±0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		−40	85	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA				0.55	
		I_{OL} = 32 mA	4.5 V			0.55	
I_I	A input	V_I = 5.5 V or GND	0 to 5.5 V			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND	3.3 V		4		pF
C_o		V_O = V_{CC} or GND	3.3 V		5		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)
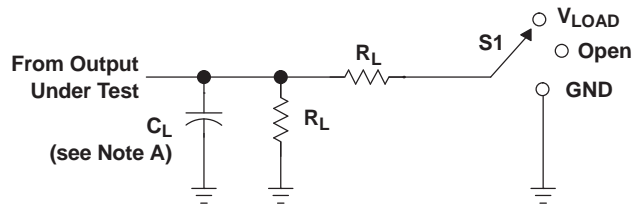
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.4	8.3	1	5.5	1.5	4.2	1	3.5	ns

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

PARAMETER MEASUREMENT INFORMATION
(OPEN DRAIN)

LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

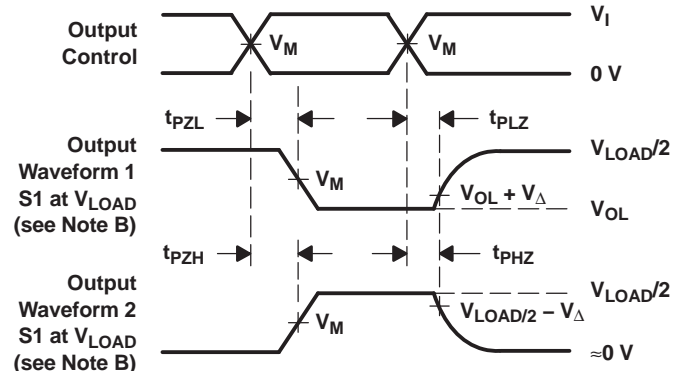| V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
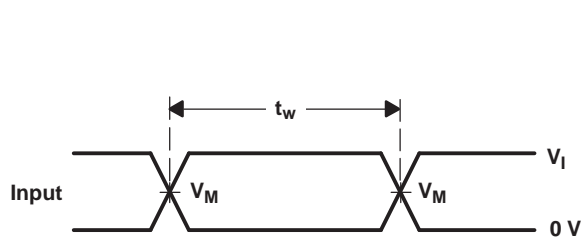
VOLTAGE WAVEFORMS
PULSE DURATION
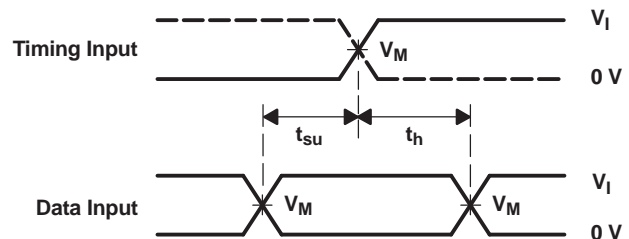
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
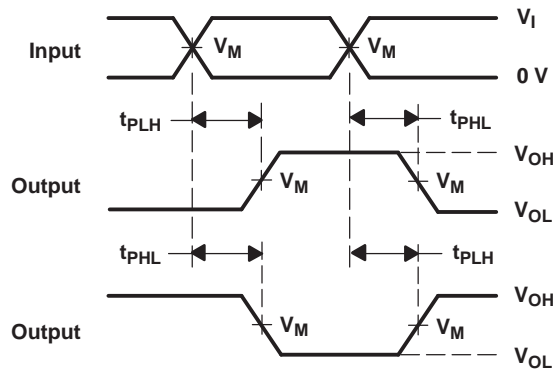
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision W (June 2008) to Revision X   **Page**

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74LVC1G07DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G07DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74LVC1G07YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74LVC1G07YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G07 :

● Automotive: SN74LVC1G07-Q1

● Enhanced Product: SN74LVC1G07-EP

NOTE: Qualified Version Definitions:

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

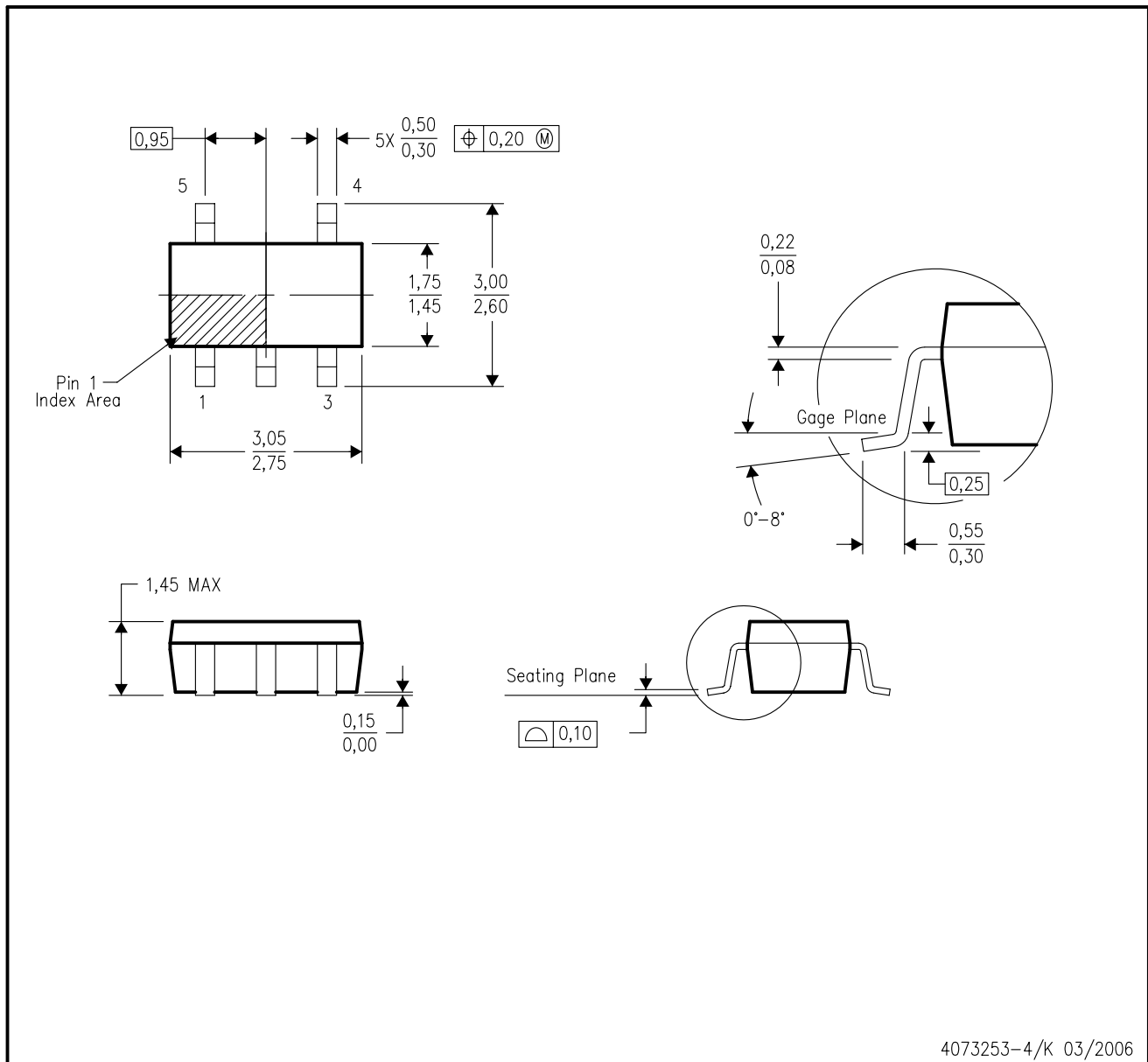| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	180.0	8.4	1.02	1.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS
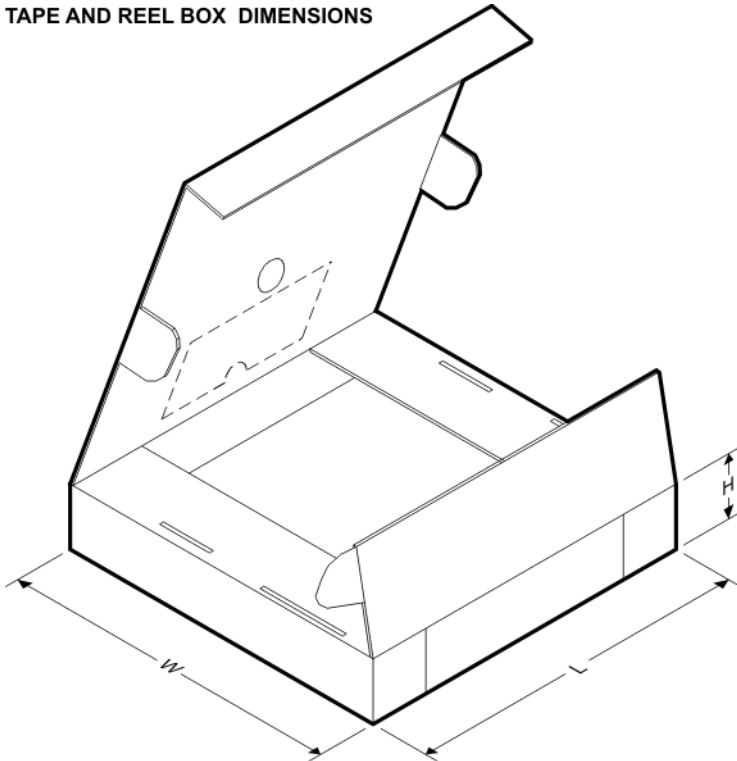
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G07DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G07DRLR	SOT	DRL	5	4000	180.0	180.0	30.0
SN74LVC1G07DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	220.0	220.0	34.0

DBV (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

0,95

5X $\frac{0,50}{0,30}$ ⊕ | 0,20 Ⓜ

5   4

$\frac{1,75}{1,45}$ $\frac{3,00}{2,60}$

Pin 1
Index Area

1   3

$\frac{3,05}{2,75}$

$\frac{0,22}{0,08}$

Gage Plane

0°−8°

0,25

$\frac{0,55}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

⌒ | 0,10

4073253−4/K 03/2006

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−178 Variation AA.

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DBV (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,90

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
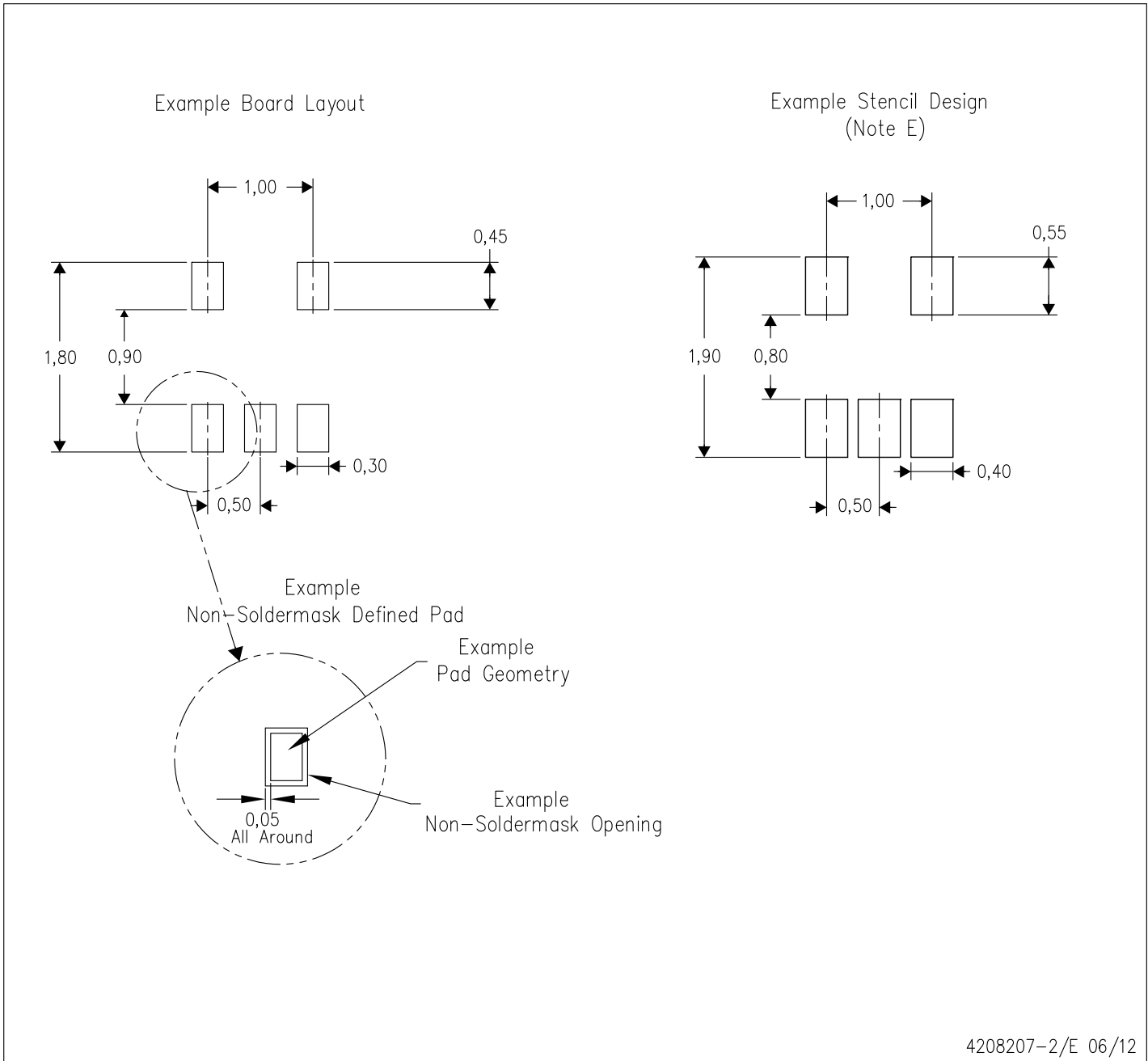All Around

4209593−3/C 08/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. Publication IPC−7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
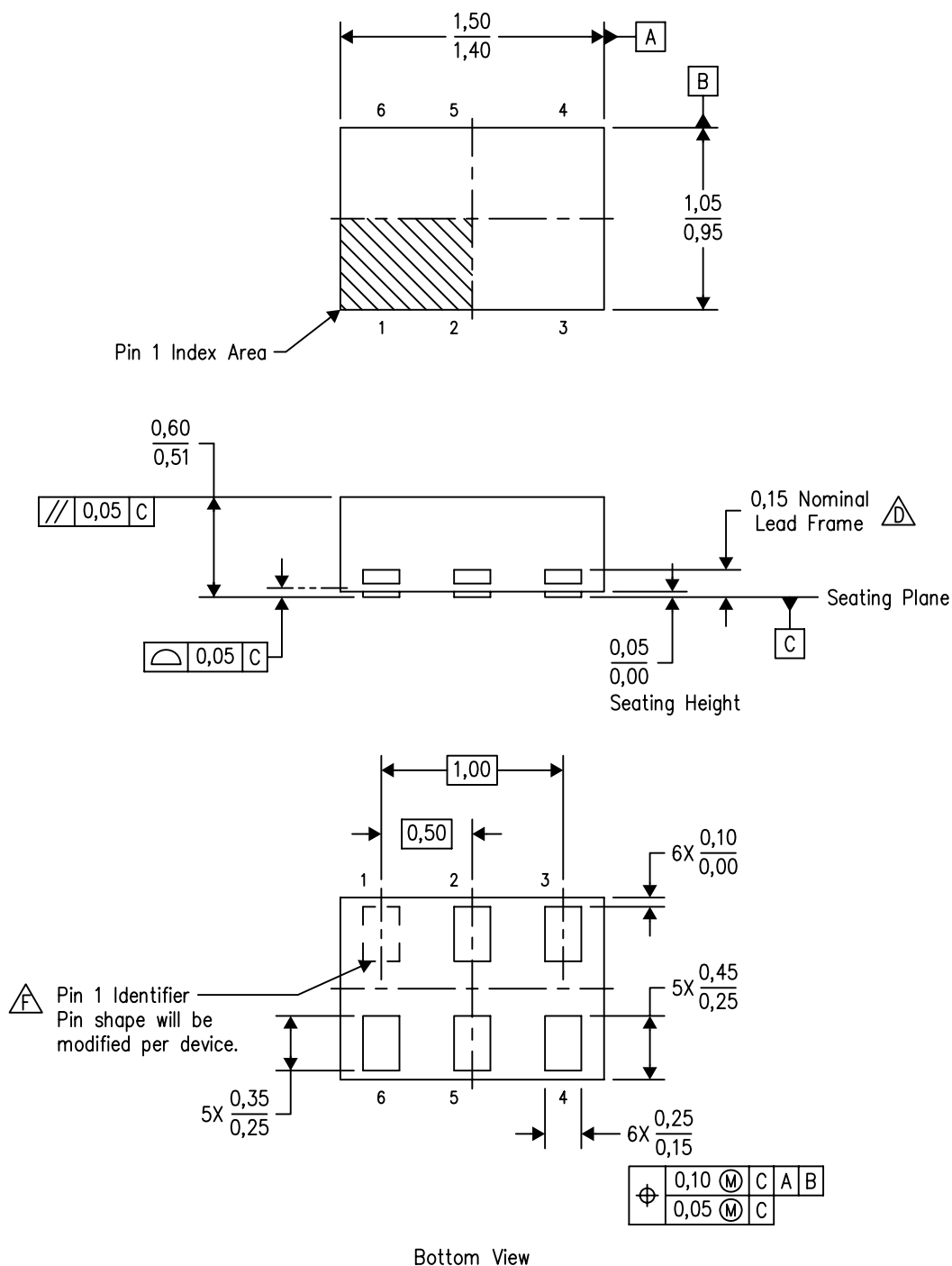   metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

2,15 / 1,85

5 4

Pin 1
Index Area

1 3

2,40 / 1,80

1,40 / 1,10

0,65

1,30

5X 0,30 / 0,15

⊕ | 0,10 Ⓜ

0,22 / 0,08

Gauge Plane
Seating Plane

0,15

0°−8°

0,46 / 0,26

1,10 / 0,80

▱ | 0,10

Seating Plane

0,10 / 0,00

4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE
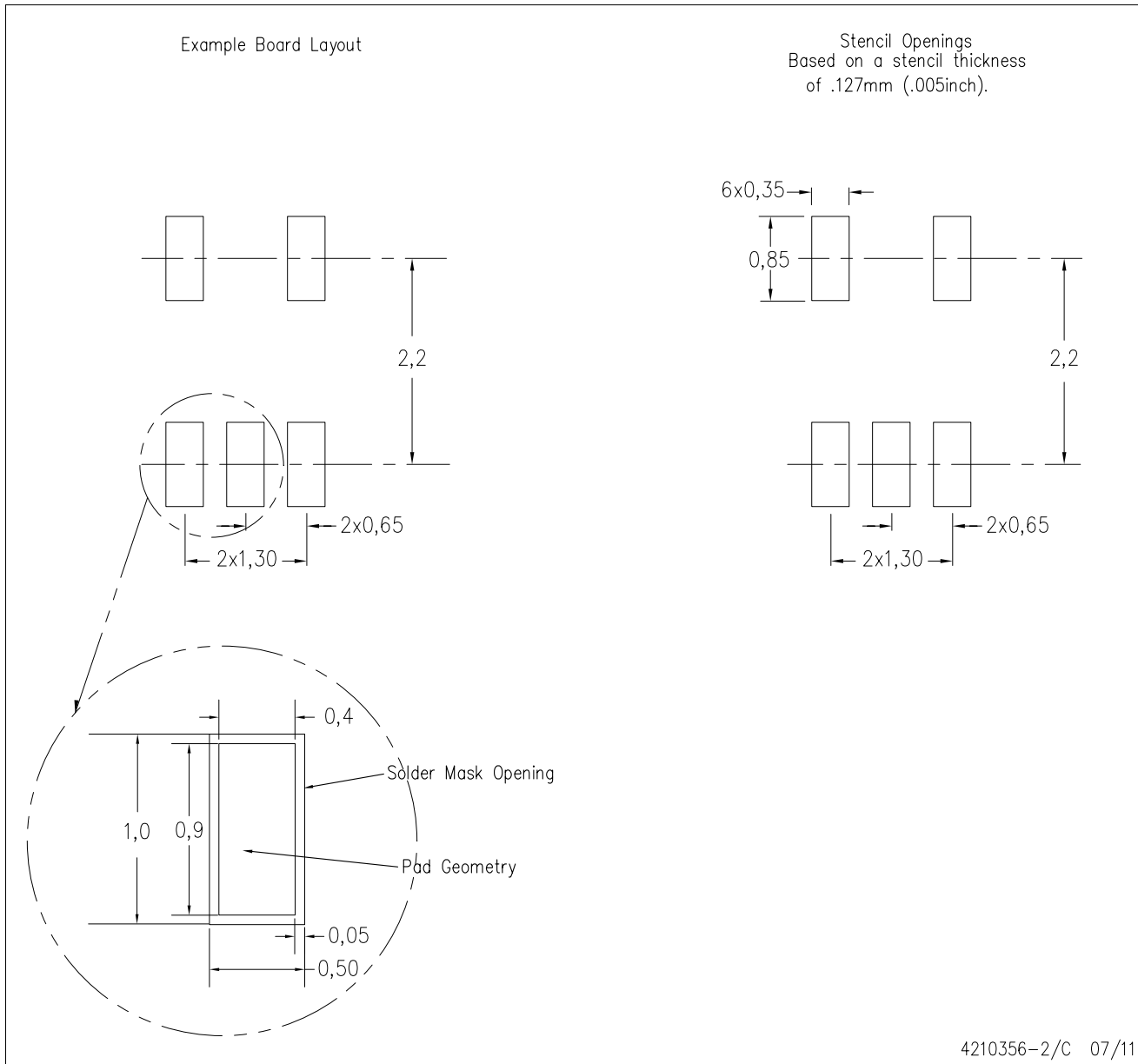
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

A

1,70
1,50

C

5X 0,27
    0,13

B

5   4

C

1,30
1,10

1,70
1,50

Pin 1 Index Area

1   2   3

0,50

5X 0,25
    0,15

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C

0,60
0,50

⌓ | 0,05 | C

Seating Plane

C

0,05
0,00

0,18
0,08

1   2   3

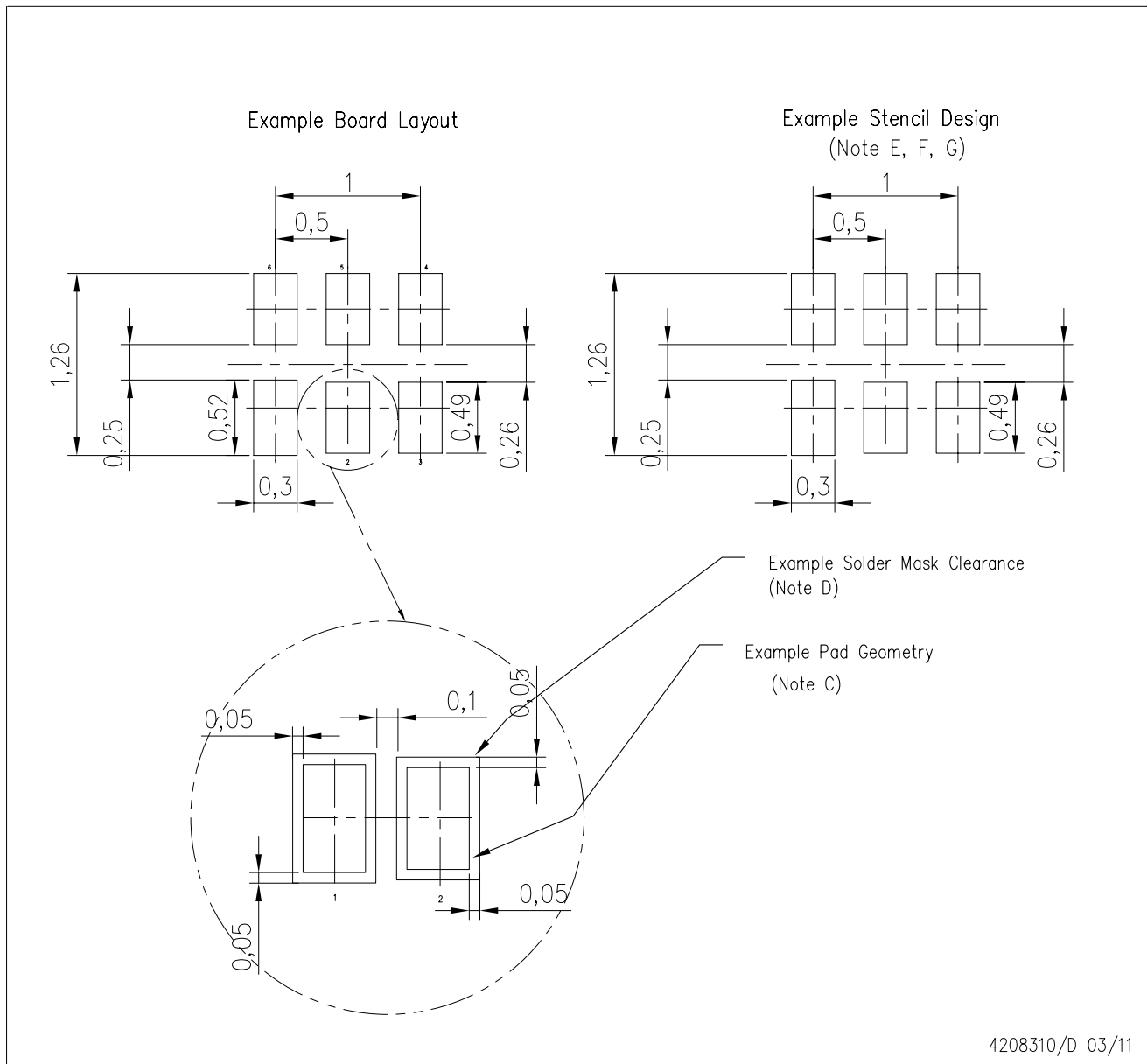5X 0,40
    0,20

5   4

Bottom View
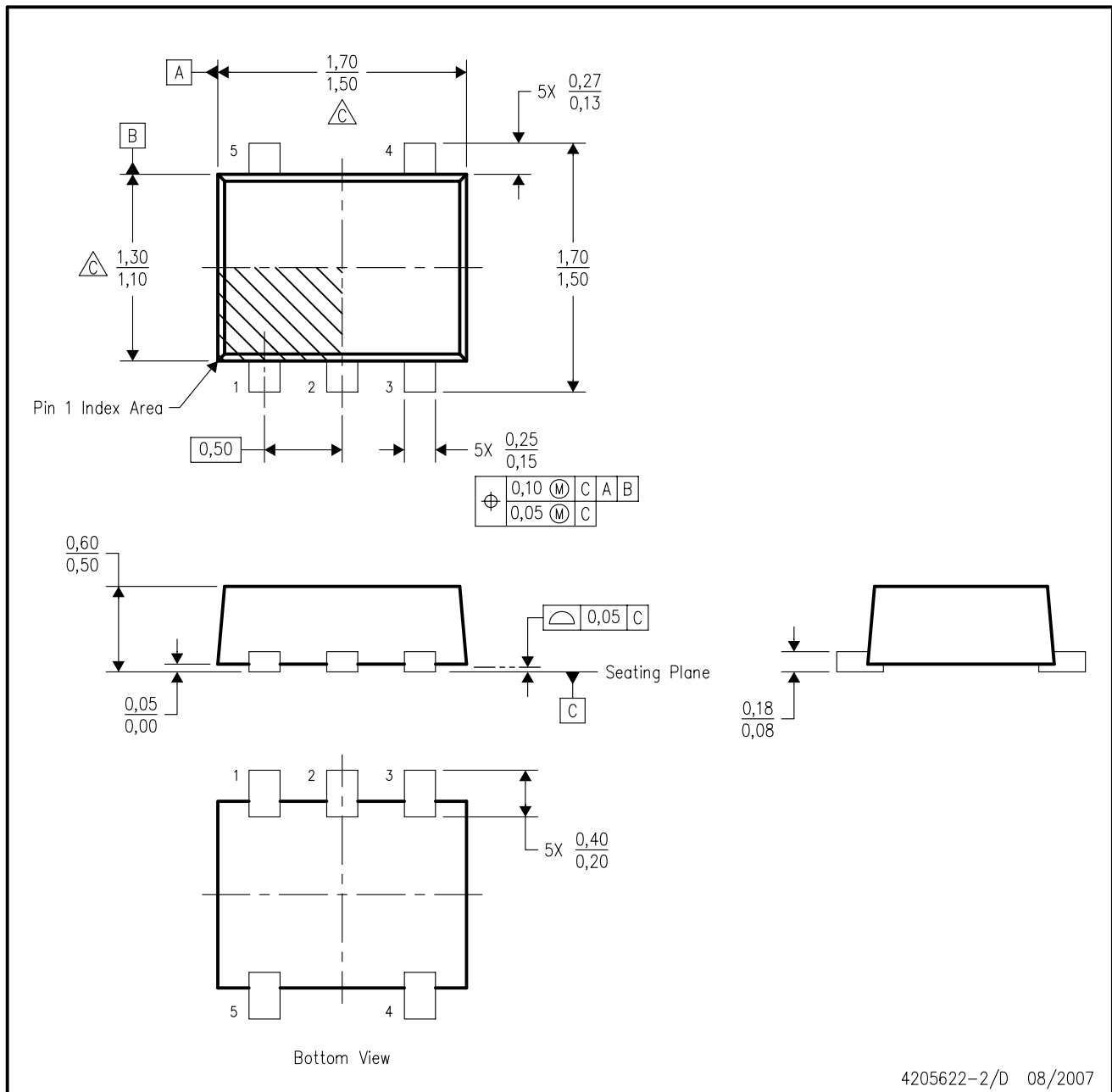
4205622−2/D   08/2007

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.
              Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
         D.   JEDEC package registration is pending.

DRL (R–PDSO–N5)   PLASTIC SMALL OUTLINE

Example Board Layout

Example Stencil Design
(Note E)

1,00

0,45

1,80   0,90

0,30

0,50

Example
Non–Soldermask Defined Pad

Example
Pad Geometry

Example
Non–Soldermask Opening

0,05
All Around

1,00

0,55

1,90   0,80

0,40

0,50

4208207–2/E 06/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
         E.   Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
              if stencil manufacturing process allows for sufficient release at smaller opening.

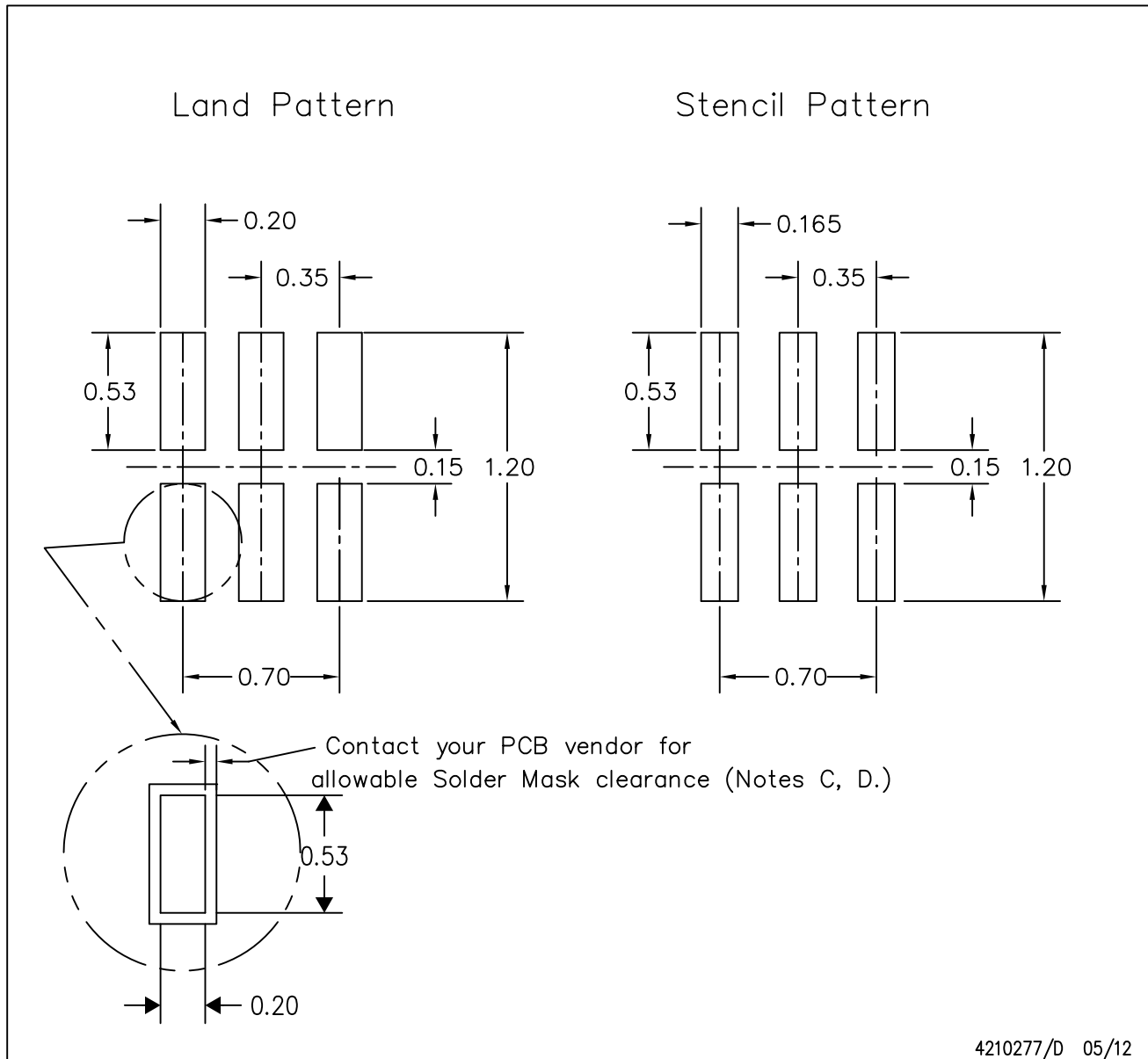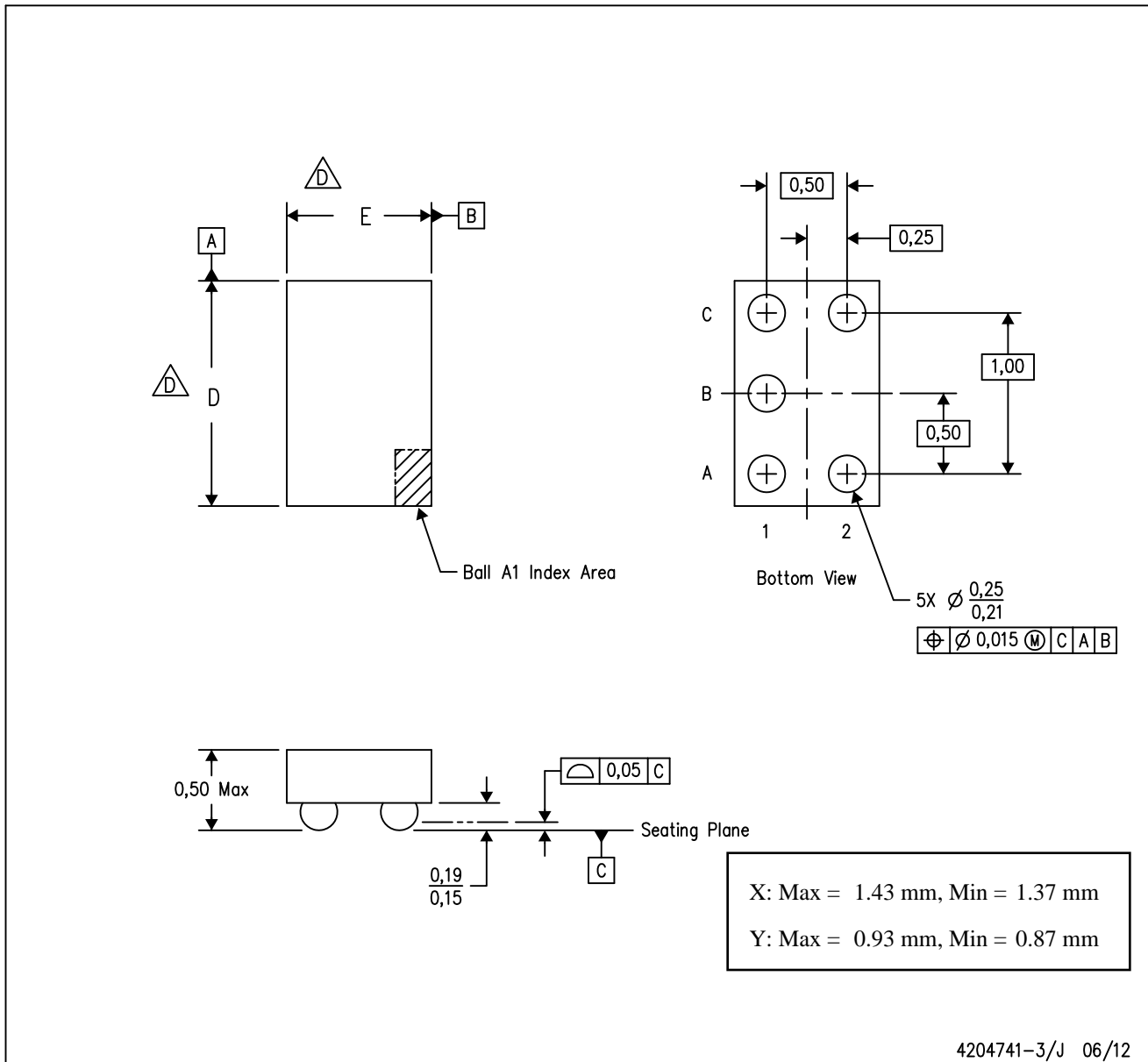DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

$\frac{1,50}{1,40}$ A

6 5 4

B

$\frac{1,05}{0,95}$

1 2 3

Pin 1 Index Area

$\frac{0,60}{0,51}$

// 0,05 C

0,15 Nominal
Lead Frame D

Seating Plane

0,05 C

$\frac{0,05}{0,00}$
Seating Height

C

1,00

0,50

1 2 3

$6X \frac{0,10}{0,00}$

F Pin 1 Identifier
Pin shape will be
modified per device.

$5X \frac{0,45}{0,25}$

$5X \frac{0,35}{0,25}$

6 5 4

$6X \frac{0,25}{0,15}$
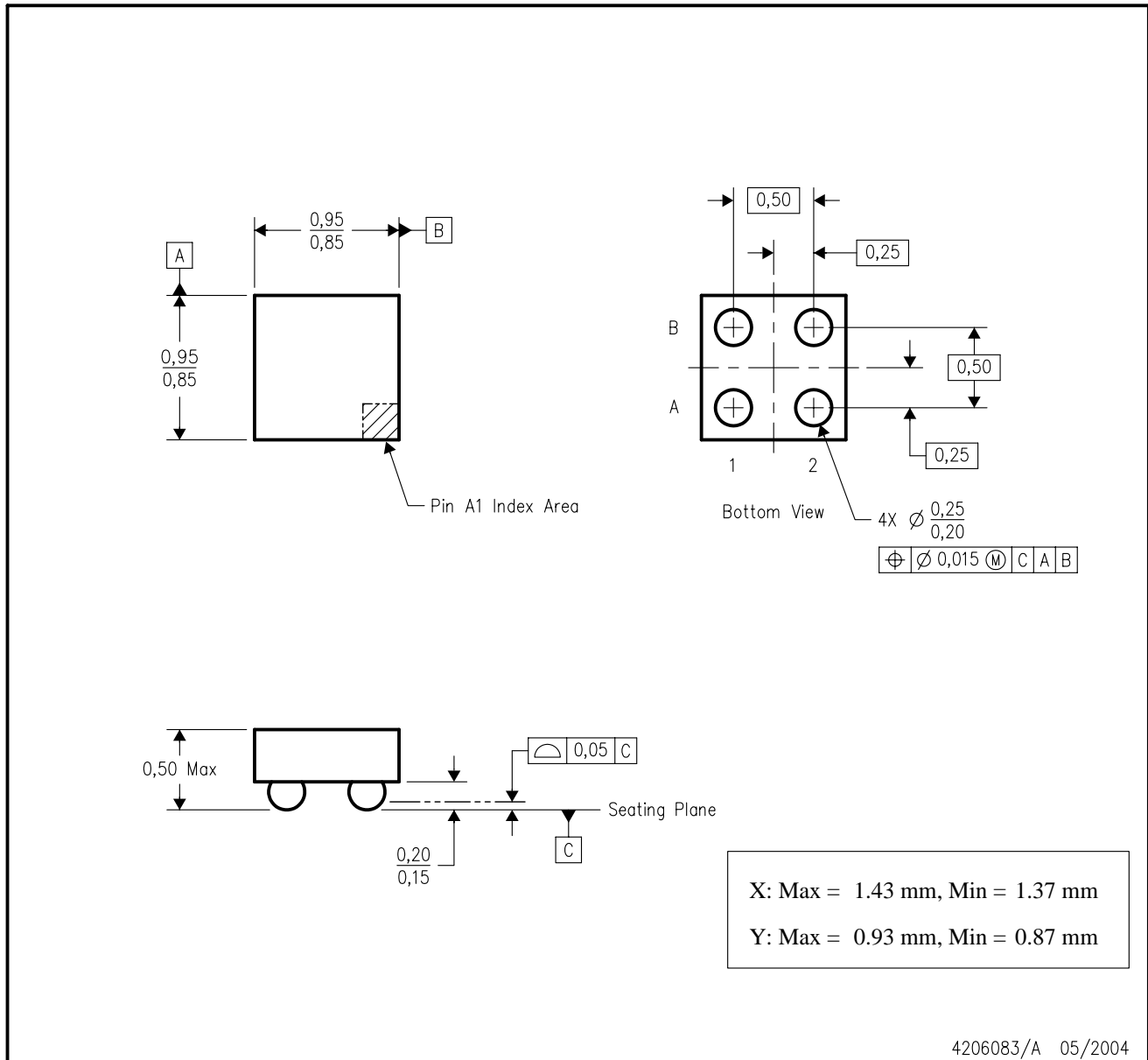
⊕ | 0,10 Ⓜ C A B
  | 0,05 Ⓜ C

Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No−Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO−287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

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DRY (S−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout   Example Stencil Design
                                                    (Note E, F, G)

Example Solder Mask Clearance
(Note D)

Example Pad Geometry
(Note C)

4208310/D 03/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
         E.   Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
              if stencil manufacturing process allows for sufficient release at smaller opening.

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DSF (S−PX2SON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

1,05
0,95

A

B

6 5 4

1,05
0,95

Pin 1 Index Area

1 2 3

0,40
0,34

0,05 C

Seating Plane

0,05
0,00

C

Seating Height

0,70

0,35

1 2 3

0,13
0,07

6X 0,45
0,35

Pin 1 Identifier

6 5 4

6X 0,20
0,14

0,07 Ⓜ C A B
0,05 Ⓜ C

Bottom View

4208186/E 03/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. SON (Small Outline No−Lead) package configuration.
         D. This package complies to JEDEC MO−287 variation X2AAF.

DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern

0.20
0.35
0.53
0.15 1.20
0.70

Stencil Pattern

0.165
0.35
0.53
0.15 1.20
0.70

Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.53

0.20

4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
    If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
    contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R−XBGA−N5)   DIE−SIZE BALL GRID ARRAY

E

A

D   D

Ball A1 Index Area

0,50

0,25

C

B

A

1   2

Bottom View

1,00

0,50

5X Ø $\frac{0,25}{0,21}$

⊕ | Ø 0,015 Ⓜ | C | A | B

0,50 Max

0,05 | C

Seating Plane

$\frac{0,19}{0,15}$

C

X: Max = 1.43 mm, Min = 1.37 mm

Y: Max = 0.93 mm, Min = 0.87 mm

4204741−3/J 06/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B. This drawing is subject to change without notice.
          C. NanoFree™ package configuration.
          D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version
              of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
          E. This package is a Pb−free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin−lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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YZV (S−XBGA−N4)   DIE−SIZE BALL GRID ARRAY

$$\frac{0,95}{0,85}$$ B

A

$$\frac{0,95}{0,85}$$

Pin A1 Index Area

0,50

0,25

B

A

1   2

Bottom View

4X $\varnothing \dfrac{0,25}{0,20}$

$\oplus \; \varnothing \; 0,015 \; Ⓜ \; C \; A \; B$

0,50

0,25

0,50 Max

$$\frac{0,20}{0,15}$$

⌒ 0,05 C

Seating Plane

C

X: Max = 1.43 mm, Min = 1.37 mm

Y: Max = 0.93 mm, Min = 0.87 mm

4206083/A   05/2004

NOTES: A.   All linear dimensions are in millimeters.
             B.   This drawing is subject to change without notice.
             C.   NanoFree™ package configuration.
             D.   This package contains lead−free balls. Refer to the 4 YEV package (drawing 4206082) for tin−lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

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