Unit: mm

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J15FV

High-Speed Switching Applications

Analog Switch Applications

· Optimum for high-density mounting in small packages

• Low on-resistance : $R_{DS(ON)} = 12 \Omega \text{ (max) (@V_{GS} = -4 V)}$

: $R_{DS(ON)} = 32 \Omega \text{ (max) } (@V_{GS} = -2.5 \text{ V})$

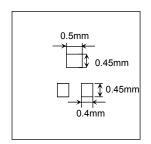
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	-30	V	
Gate-Source voltage		V _{GSS}	±20	٧	
Drain current	DC	I _D	-100	mA	
	Pulse	I _{DP}	-200		
Power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm \times 25.4 mm \times 1.6 mm, Cu Pad: 0.585 mm²)



1.2±0.05 0.8±0.05 1.340.05 1.340.05 1.340.05 1.340.05 1.340.05 2.300RCE 3.DRAIN

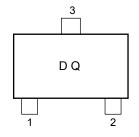
2-1L1B

Weight: 1.5 mg (typ.)

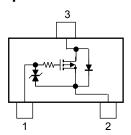
JEITA

TOSHIBA

Marking



Equivalent Circuit (top view)



Handling Precaution

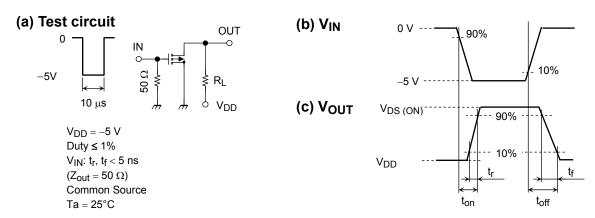
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	MIN	TYP.	MAX	UNIT	
Gate leakage current		I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	_		V	
Drain cut-off current		I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$		_	-1	μΑ	
Gate threshold voltage		V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-1.1	_	-1.7	>	
Forward transfer admittance		Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA (Note 2)}$	20	_		mS	
Drain-Source on-resistance		R _{DS (ON)}	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V (Note 2)}$		8	12	Ω	
			$I_D = -1 \text{ mA}, V_{GS} = -2.5 \text{ V (Note 2)}$		14	32		
Input capacitance		C _{iss}			9.1		pF	
Reverse transfer capacitance		C _{rss}	$V_{DS} = -3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		3.5		pF	
Output capacitance		Coss			8.6		pF	
Switching time	Turn-on time	t _{on}	$V_{DD} = -5 \text{ V}, I_{D} = -10 \text{ mA},$		65		ns	
	Turn-off time	t _{off}	$V_{GS} = 0 \text{ to } -5 \text{ V}$		175	_		

Note 2: Pulse Test

Switching Time Test Circuit

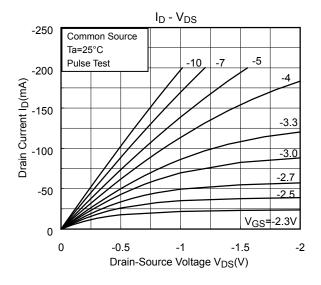


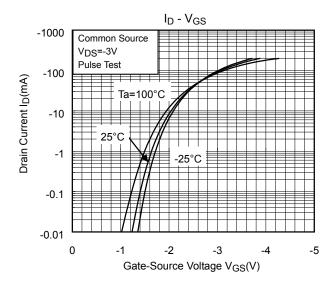
Precaution

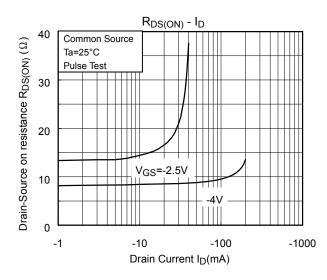
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -100 μ A for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} .

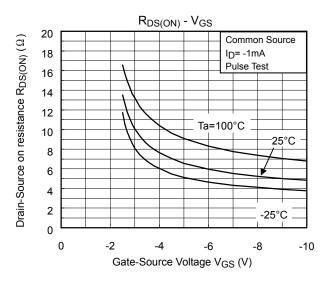
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

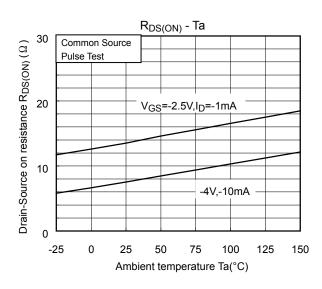
Please take this into consideration when using the device.

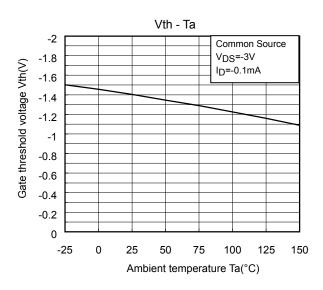


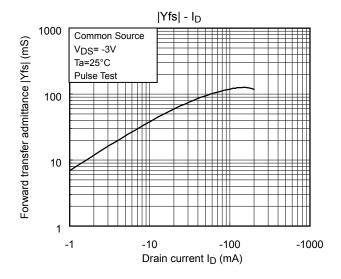


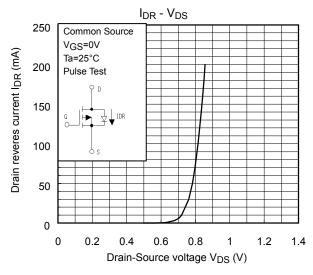


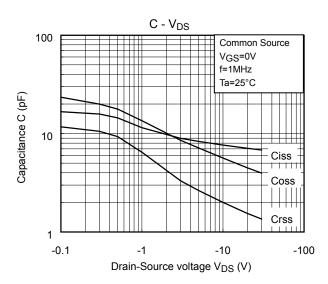


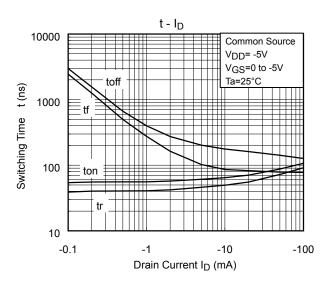


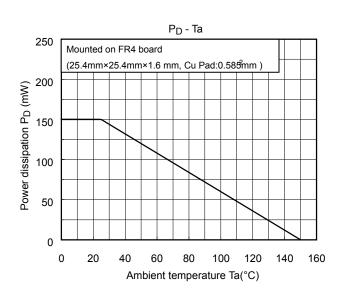












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