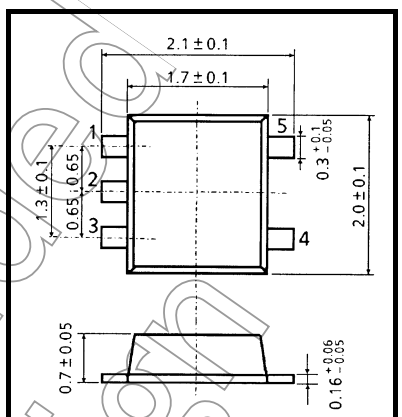
Silicon N Channel MOS Type / Silicon Epitaxial Planer Diode

SSM5H90TU

High-Speed Switching Applications

- Integrates an N-ch MOSFET and planer diodes into one package.
- Low $R_{DS\ (ON)}$ and low V_F

Unit: mm



UFV

JEDEC	—
JEITA	—
TOSHIBA	2-2R1A

Weight: 7 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C) for the MOSFET

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	20	V
Gate-Source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	2.4	A
	Pulse	I_{DP} (Note 2)	4.8	
Drain power dissipation		P_D (Note 1)	0.5	W
		t = 10s	0.8	
Channel temperature		T_{ch}	150	°C

Absolute Maximum Ratings (Ta = 25°C) for the Diodes

Characteristics	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	300	mA
Average forward current	I_O	100	mA
Surge current (10ms)	I_{FSM}	2	A
Junction temperature	T_j	125	°C

Absolute Maximum Ratings (Ta = 25°C) for the MOSFET and Diodes

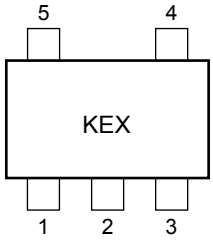
Characteristics	Symbol	Rating	Unit
Storage temperature	T_{stg}	−55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

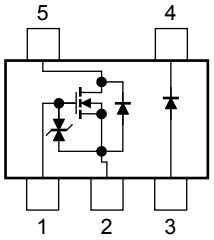
Note 1: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Note 2: Puls width limited by max channel temperature

Marking



Equivalent Circuit



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing and use containers and other objects that are made of anti-static materials.

The Channel-to-Ambient thermal resistance $R_{th\ (ch\text{-}a)}$ and the drain power dissipation P_D vary according to the board material, board area, board thickness and pad area. When using this device, please take heat dissipation fully into account.

MOSFET

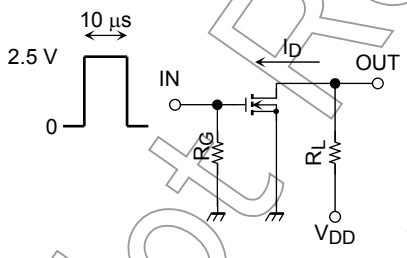
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0 V		20	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = − 10 V		12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 10 V, V_{DS} = 0 V		—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA		0.35	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 1.0 A	(Note 3)	3.5	7	—	S
Drain-Source ON-resistance		$R_{DS\ (ON)}$	I_D = 1.5 A, V_{GS} = 4.0 V	(Note 3)	—	53	65	mΩ
			I_D = 1.5 A, V_{GS} = 2.5 V	(Note 3)	—	63	80	
			I_D = 1.0 A, V_{GS} = 1.8 V	(Note 3)	—	77	110	
			I_D = 0.5 A, V_{GS} = 1.5 V	(Note 3)	—	92	157	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		—	400	—	pF
Output capacitance		C_{oss}			—	68	—	
Reverse transfer capacitance		C_{rss}			—	60	—	
Total Gate Charge		Q_g	V_{DS} = 10 V, I_{DS} = 2.4 A V_{GS} = 4 V		—	6.3	—	nC
Gate−Source Charge		Q_{gs}			—	4.3	—	
Gate−Drain Charge		Q_{gd}			—	2.0	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 2 A, V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω		—	14	—	ns
	Turn-off time	t_{off}			—	15	—	
Drain-Source forward voltage		V_{DSF}	I_D = −2.4 A, V_{GS} = 0 V	(Note 3)	—	−0.85	-1.2	V

Note 3: Pulse measurement

Switching Time Test Circuit

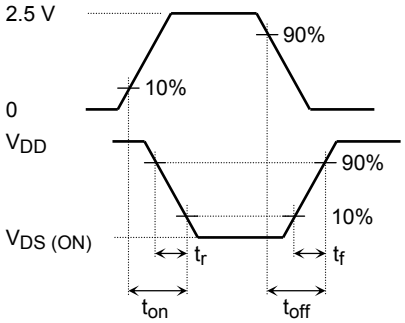
(a)Test circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the SSM5H90TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

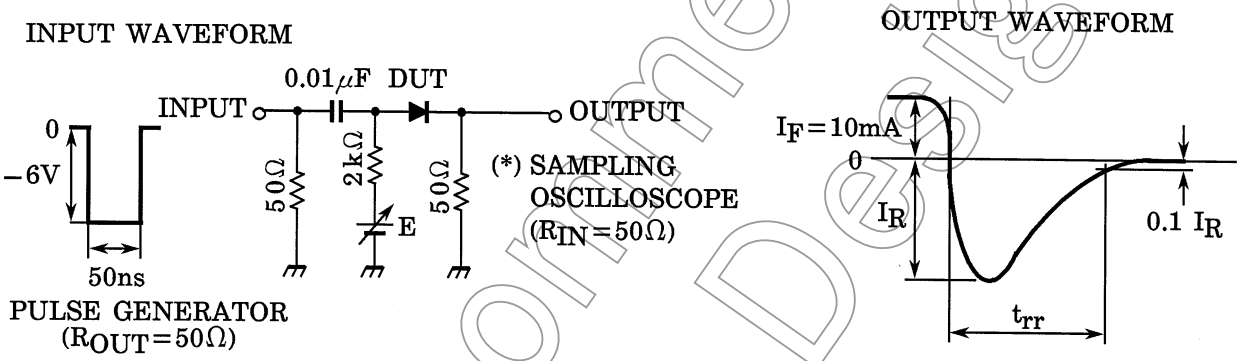
Take this into consideration when using the device.

Planer Diodes

Electrical Characteristics (Ta = 25°C)

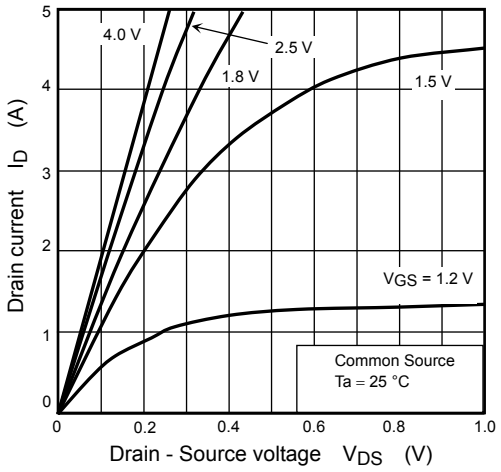
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_{F\ (1)}$	I_F = 1mA	—	0.60	—	V
	$V_{F\ (2)}$	I_F = 10mA	—	0.72	—	
	$V_{F\ (3)}$	I_F = 100mA	—	0.90	1.20	
Reverse current	$I_{R\ (1)}$	V_R = 30V	—	—	0.1	μA
	$I_{R\ (2)}$	V_R = 80V	—	—	0.5	
Total capacitance	C_T	V_R = 0, f = 1MHz	—	0.9	—	pF
Reverse recovery time	t_{rr}	I_F = 10mA (Note.4)	—	1.6	—	ns

Note 4: Reverse recovery time (t_{rr}) test circuit

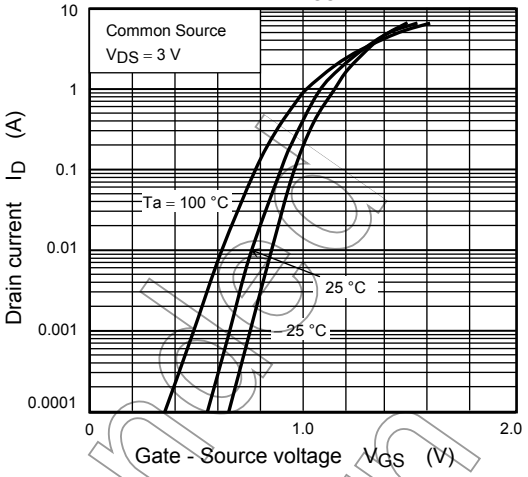


Electrical Characteristics Graph for the MOSFET

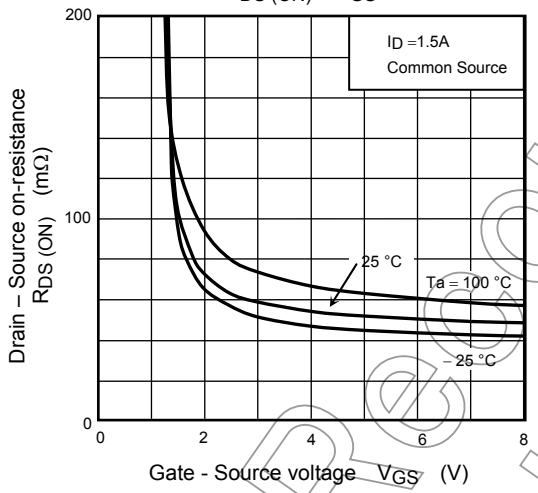
$I_D - V_{DS}$



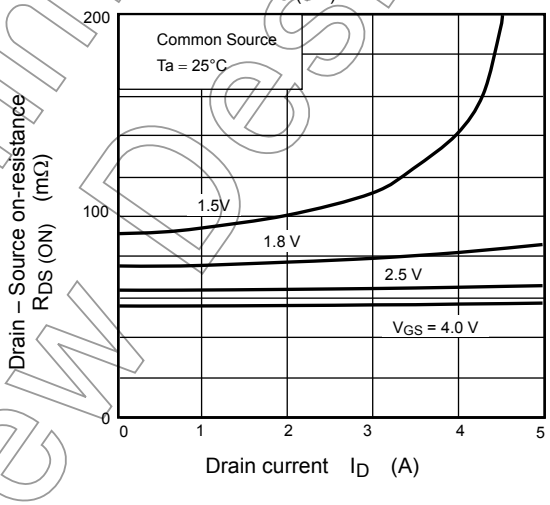
$I_D - V_{GS}$



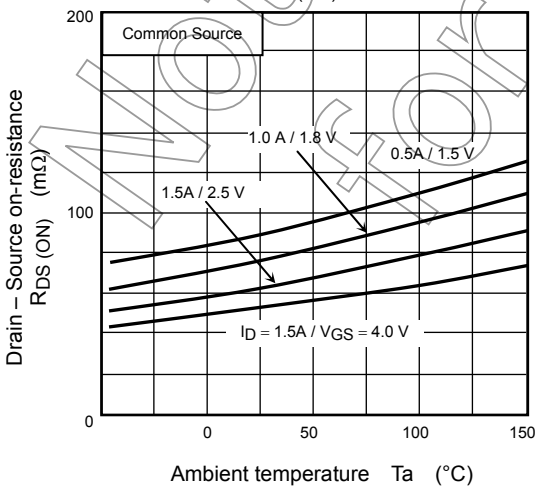
$R_{DS\ (ON)} - V_{GS}$



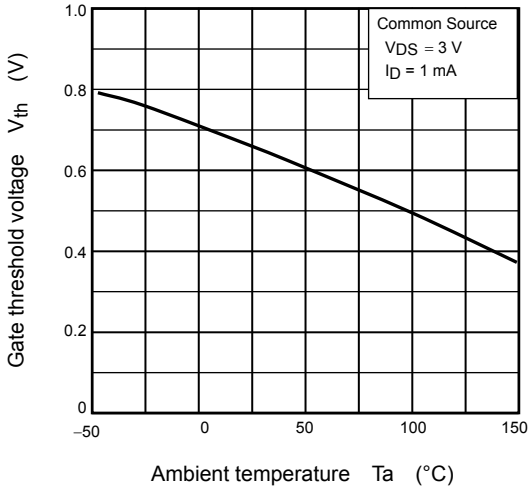
$R_{DS\ (ON)} - I_D$



$R_{DS\ (ON)} - Ta$

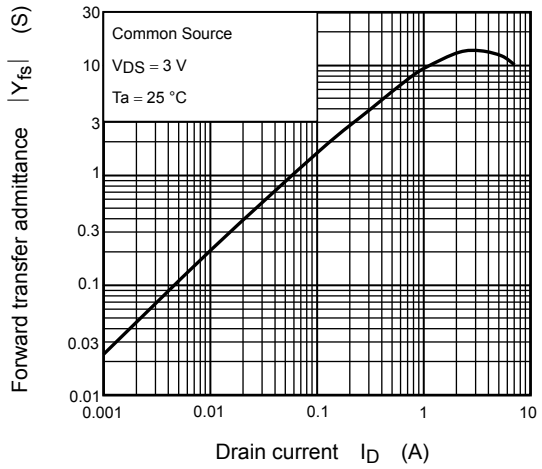


$V_{th} - Ta$

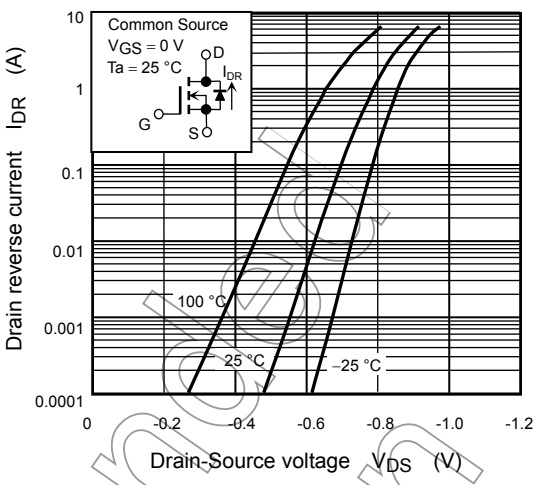


Electrical Characteristics Graph for the MOSFET

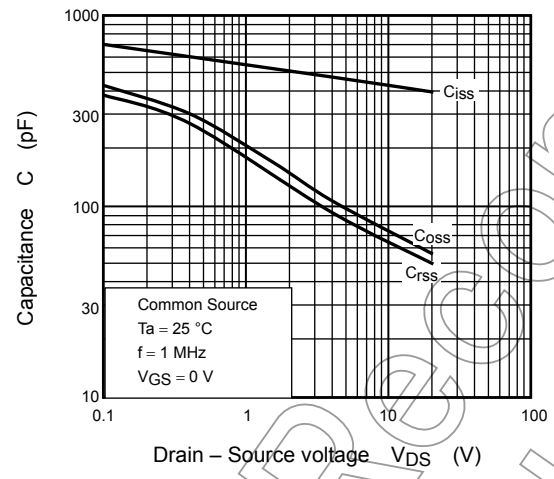
$|Y_{fs}| - I_D$



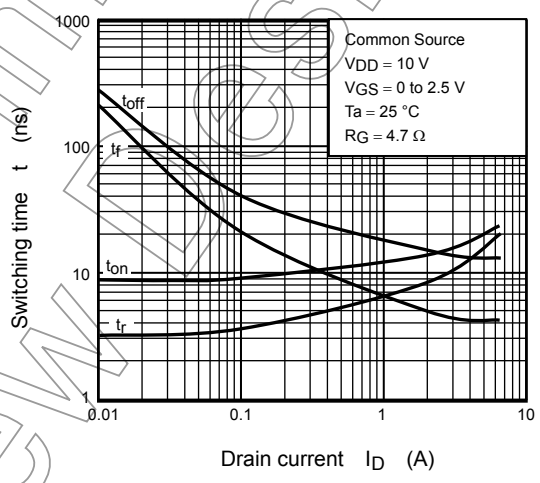
$I_{DR} - V_{DS}$



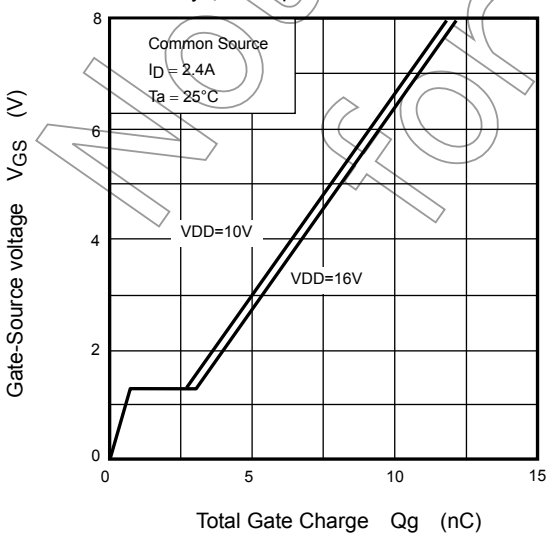
$C - V_{DS}$



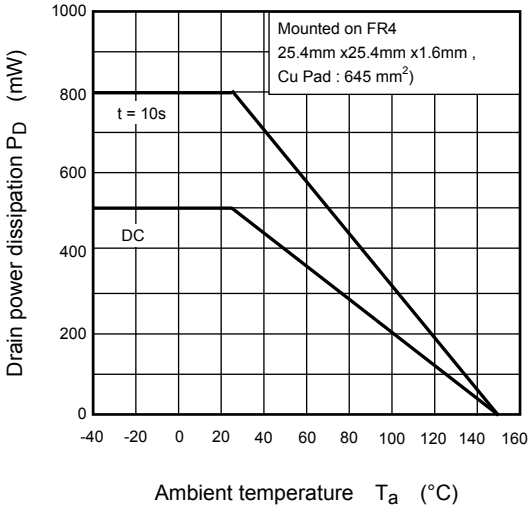
$t - I_D$



Dynamic Input Characteristic

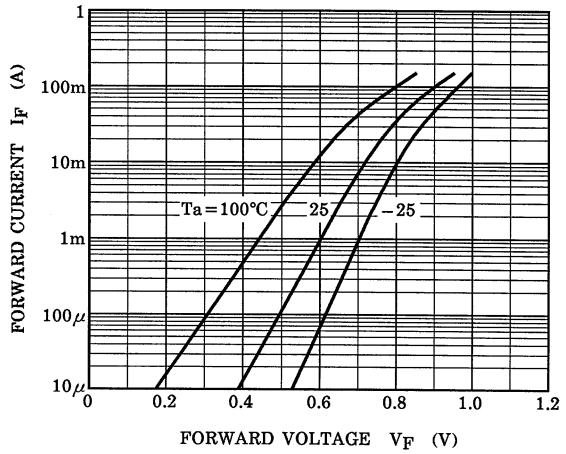


$P_D - T_a$

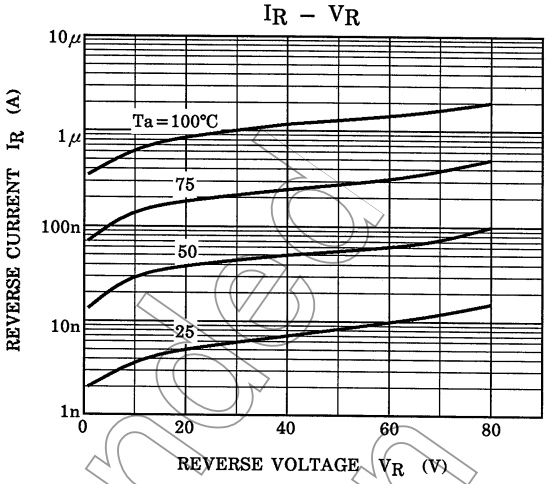


Electrical Characteristics Graph for the Planer Diodes

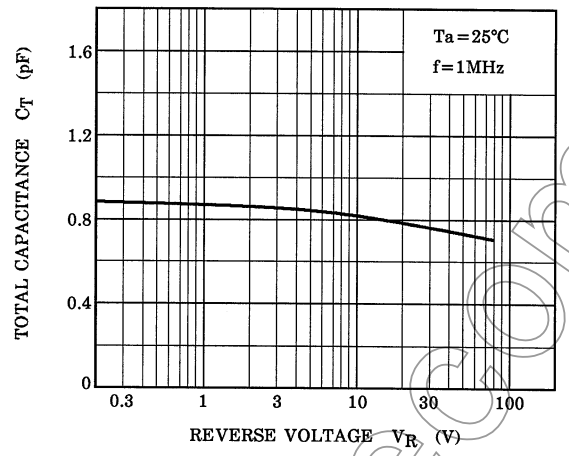
$I_F - V_F$



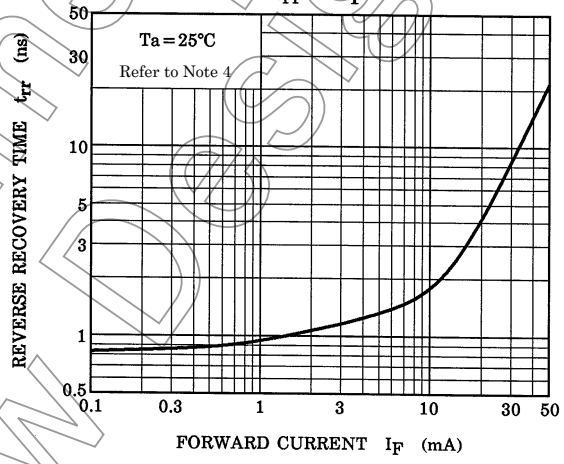
$I_R - V_R$



$C_T - V_R$



$t_{rr} - I_F$



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