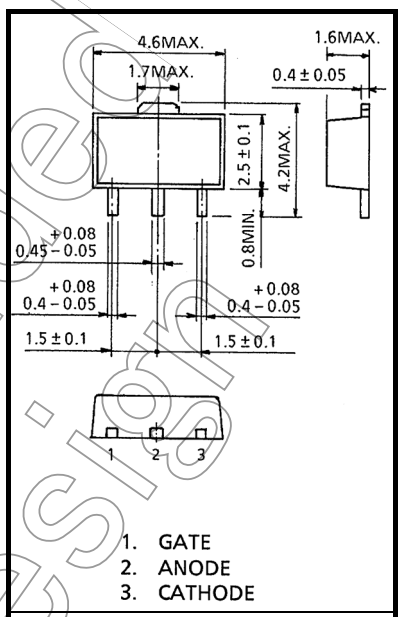
TOSHIBA THYRISTOR SILICON PLANAR TYPE

URSF05G49-1P, URSF05G49-3P, URSF05G49-5P

LOW POWER SWITCHING AND CONTROL APPLICATIONS

- Repetitive Peak Off−State Voltage: V_{DRM} = 400 V
  Repetitive Peak Reverse Voltage: V_{RRM} = 400 V
- Average On−State Current: $I_{T\ (AV)}$ = 500 mA
- Reduce a Quantity of Parts and Manufacturing Process Because of Built−in R_{GK}: R_{GK} = 1kΩ, 2.7kΩ, 5.1kΩ (Typ.)

Unit: mm



1. GATE
2. ANODE
3. CATHODE

JEDEC	—
JEITA	—
TOSHIBA	13-5B1A

Weight: 0.2 g (typ.)

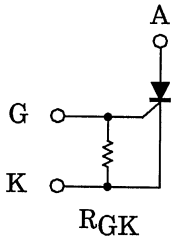
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
Repetitive Peak Off−State Voltage and Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}	400	V
Non−Repetitive Peak Reverse Voltage (Non−Repetitive<5ms, T_j = 0~125°C)	V_{RSM}	500	V
Average On−State Current (Half Sine Waveform)	$I_{T\ (AV)}$	500	mA
R.M.S On−State Current	$I_{T\ (RMS)}$	800	mA
Peak One Cycle Surge On−State Current (Non−Repetitive)	I_{TSM}	9 (50Hz)	A
		10 (60Hz)	
I^2t Limit Value	I^2t	0.4	A^2s
Critical Rate of Rise of On−State Current (Note 1)	di / dt	10	A / μs
Peak Gate Power Dissipation	P_{GM}	0.1	W
Average Gate Power Dissipation	$P_{G(AV)}$	0.01	W
Peak Forward Gate Voltage	V_{FGM}	3.5	V
Peak Reverse Gate Voltage	V_{RGM}	−5	V
Peak Forward Gate Current	I_{GM}	125	mA
Junction Temperature	T_j	−40~125	°C
Storage Temperature Range	T_{stg}	−40~125	°C

Note 1: di / dt Test condition
i_G = 5mA, t_{gw}=10μs,
t_{gr}≤250ns

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

EQUIVALENT CIRCUIT

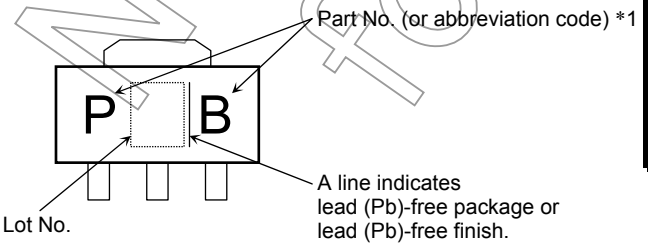


ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current		I_{DRM} I_{RRM}	V_{DRM} = V_{RRM} = Rated	—	—	10	μA
Peak On−State Voltage		V_{TM}	I_{TM} = 1A	—	—	1.5	V
Gate Trigger Voltage		V_{GT}	V_D = 6V, R_L = 100Ω	—	—	0.8	V
Gate Trigger Current	URSF05G49−1P	I_{GT}	V_D = 6V, R_L = 100Ω	250	700	1000	μA
	URSF05G49−3P			100	250	400	
	URSF05G49−5P			50	160	250	
Holding Current	URSF05G49−1P	I_H	I_{TM} = 500mA, V_D = 6V	—	—	6	mA
	URSF05G49−3P			—	—	3	
	URSF05G49−5P			—	—	2	
Resistor Between Gate and Cathode	URSF05G49−1P	R_{GK}	—	700	1000	1300	Ω
	URSF05G49−3P			1890	2700	3510	
	URSF05G49−5P			3570	5100	6630	
Critical Rate of Rise of Off-State Voltage	URSF05G49−1P	d_V / dt	V_{DRM} = Rated, Exponential Rise	—	200	—	V / μs
	URSF05G49−3P			—	70	—	
	URSF05G49−5P			—	40	—	
Turn−On Time		t_{gt}	V_D = Rated, i_G = 5mA	—	—	1.5	μs
Thermal Resistance		$R_{th\ (j-a)}$	Junction to Ambient	—	—	70	°C / W

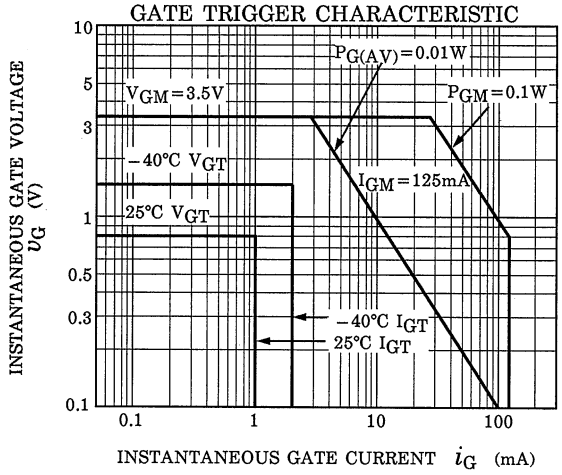
Note: Thermal Resistance Test Condition
Use 0.6×30×30mm Alumina Plate

MARKING

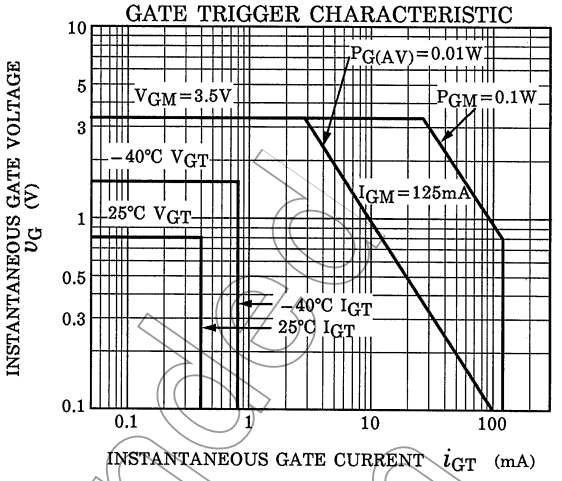


	Part No. (or abbreviation code)	Part No.
*1	PB	URSF05G49-1P
	PC	URSF05G49-3P
	PD	URSF05G49-5P

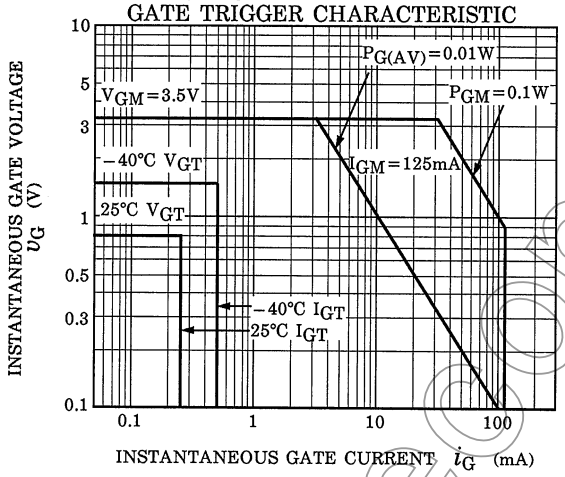
URSF05G49–1P
GATE TRIGGER CHARACTERISTIC



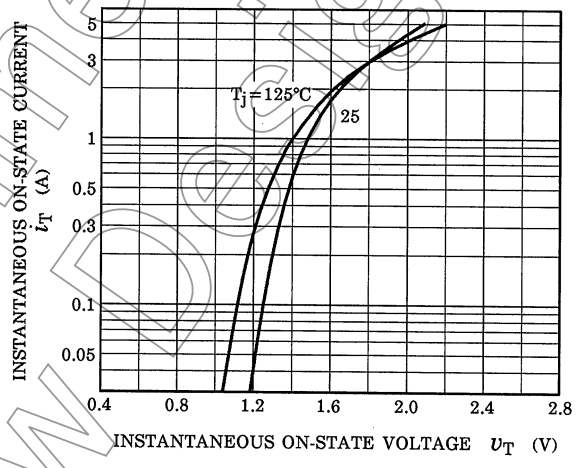
URSF05G49–3P
GATE TRIGGER CHARACTERISTIC



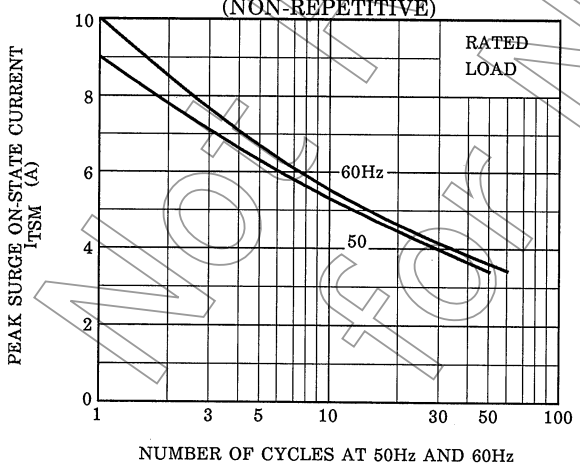
URSF05G49–5P
GATE TRIGGER CHARACTERISTIC



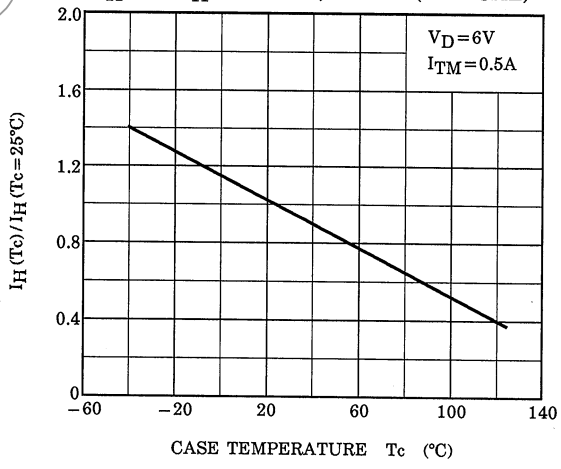
$i_T - v_T$



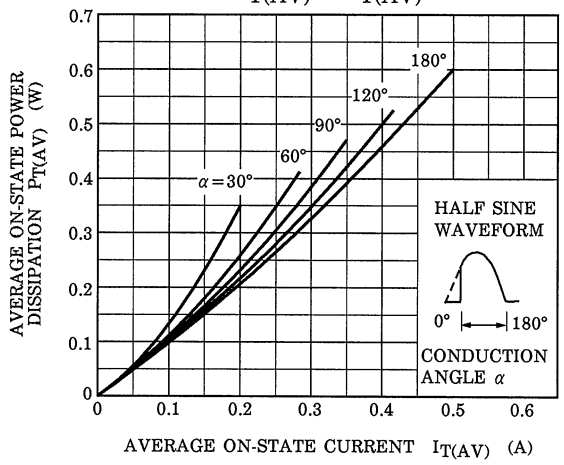
SURGE ON-STATE CURRENT
(NON-REPETITIVE)



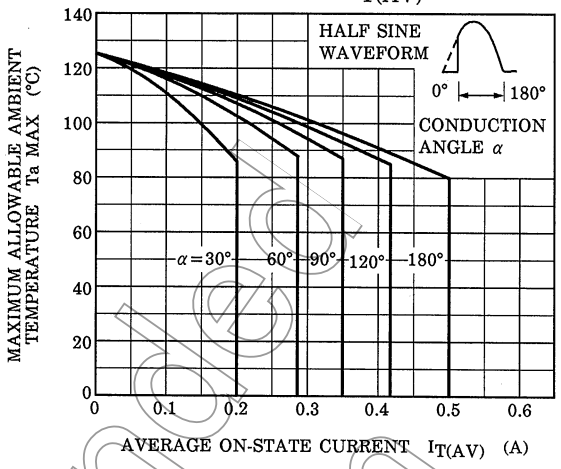
I_H (Tc) / I_H 9Tc=25°C) − Tc (TYPICAL)



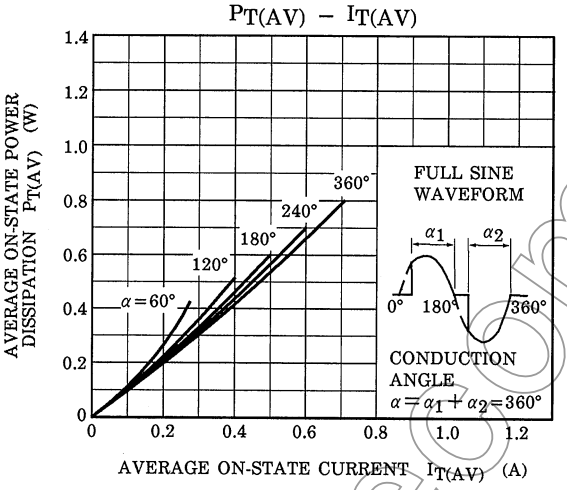
$P_{T(AV)} - I_{T(AV)}$



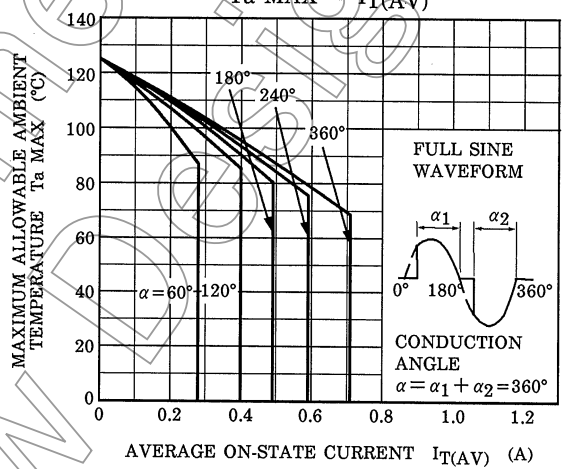
Ta MAX – $I_{T(AV)}$



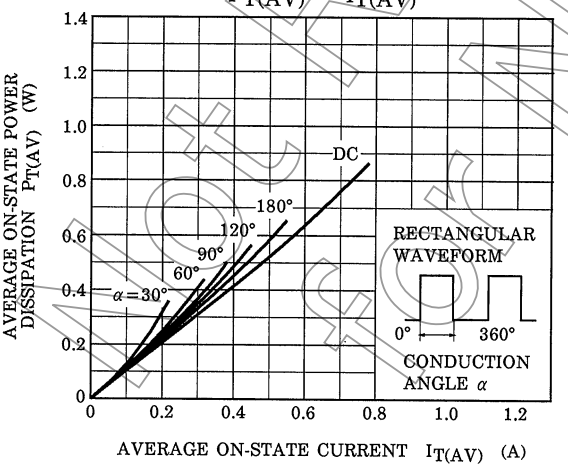
$P_{T(AV)} - I_{T(AV)}$



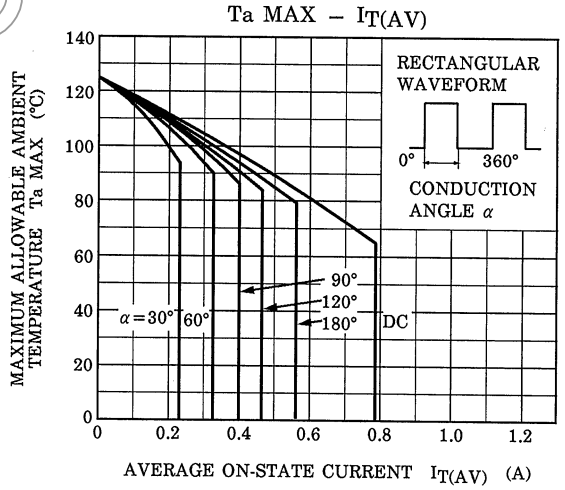
Ta MAX – $I_{T(AV)}$



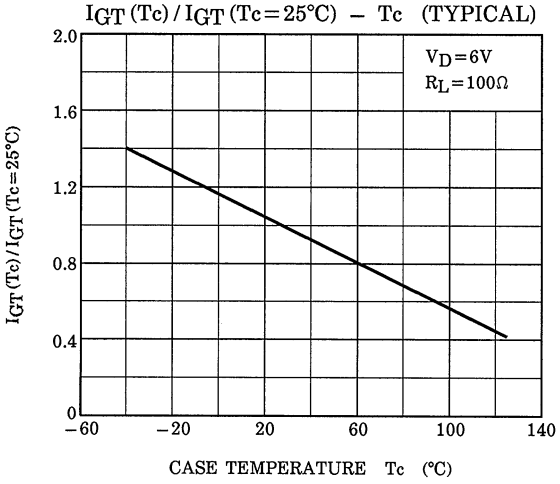
$P_{T(AV)} - I_{T(AV)}$



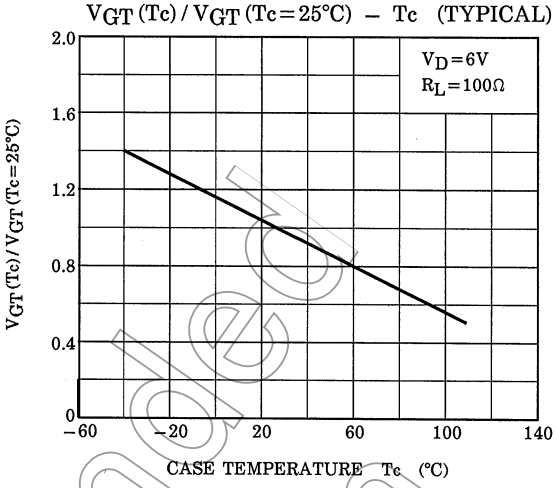
Ta MAX – $I_{T(AV)}$



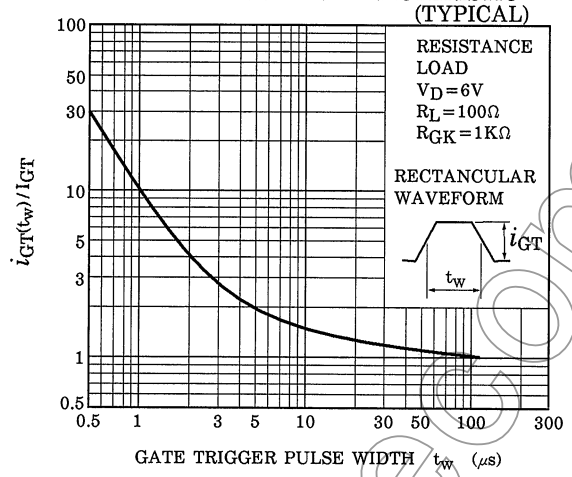
I_{GT} (Tc) / I_{GT} (Tc = 25°C) – Tc (TYPICAL)



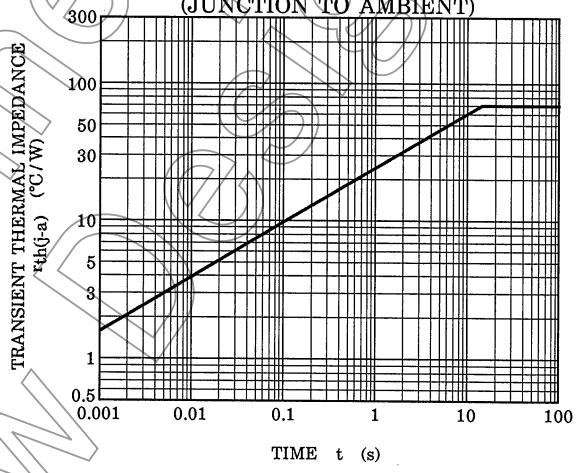
V_{GT} (Tc) / V_{GT} (Tc = 25°C) – Tc (TYPICAL)



PULSE TRIGGER CHARACTERISTIC (TYPICAL)



TRANSIENT THERMAL IMPEDANCE (JUNCTION TO AMBIENT)



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