

# DATA SHEET

**PEMD2; PIMD2; PUMD2**  
NPN/PNP resistor-equipped  
transistors; R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$

Product specification  
Supersedes data of 2003 Jun 06

2004 Apr 21

## NPN/PNP resistor-equipped transistors; R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$

## PEMD2; PIMD2; PUMD2

### FEATURES

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	50	V
I <sub>O</sub>	output current (DC)	–	100	mA
TR1	NPN (PIMD2: PNP)	–	–	–
TR2	PNP (PIMD2: NPN)	–	–	–
R1	bias resistor	22	–	k $\Omega$
R2	bias resistor	22	–	k $\Omega$

### DESCRIPTION

NPN/PNP resistor-equipped transistors (see "Simplified outline, symbol and pinning" for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/NPN COMPLEMENT
	PHILIPS	EIAJ			
PEMD2	SOT666	–	D4	PEMB1	PEMH1
PIMD2	SOT457	SC-74	M5	–	–
PUMD2	SOT363	SC-88	D*2 <sup>(1)</sup>	PUMB1	PUMH1

### Note

- \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

NPN/PNP resistor-equipped transistors;  
 R1 = 22 kΩ, R2 = 22 kΩ

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**SIMPLIFIED OUTLINE, SYMBOL AND PINNING**

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD2 PUMD2		1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1
PIMD2		1	emitter TR2
		2	base TR2
		3	collector TR1
		4	emitter TR1
		5	base TR1
		6	collector TR2

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD2	–	plastic surface mounted package; 6 leads	SOT666
PIMD2	–	plastic surface mounted package; 6 leads	SOT457
PUMD2	–	plastic surface mounted package; 6 leads	SOT363

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage TR1 positive negative		–	+40	V
			–	–10	V
V <sub>I</sub>	input voltage TR2 positive negative		–	+10	V
			–	–40	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT363	note 1	–	200	mW
	SOT457	note 1	–	300	mW
	SOT666	notes 1 and 2	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT363	note 1	–	300	mW
	SOT457	note 1	–	600	mW
	SOT666	notes 1 and 2	–	300	mW

### Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.

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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per transistor</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C		
	SOT363	note 1	625	K/W
	SOT457	note 1	417	K/W
	SOT666	notes 1 and 2	625	K/W
<b>Per device</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C		
	SOT363	note 1	416	K/W
	SOT457	note 1	208	K/W
	SOT666	notes 1 and 2	416	K/W

### Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.

### CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	–	–	1	μA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	–	–	50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	–	–	180	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA	60	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	–	–	150	V
V <sub>i(off)</sub>	input-off voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA	–	1.1	0.8	V
V <sub>i(on)</sub>	input-on voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 5 mA	2.5	1.7	–	V
R1	input resistor		15.4	22	28.6	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz				
	TR1 (NPN) TR2 (PNP)		– –	– –	2.5 3	pF pF

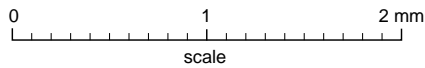
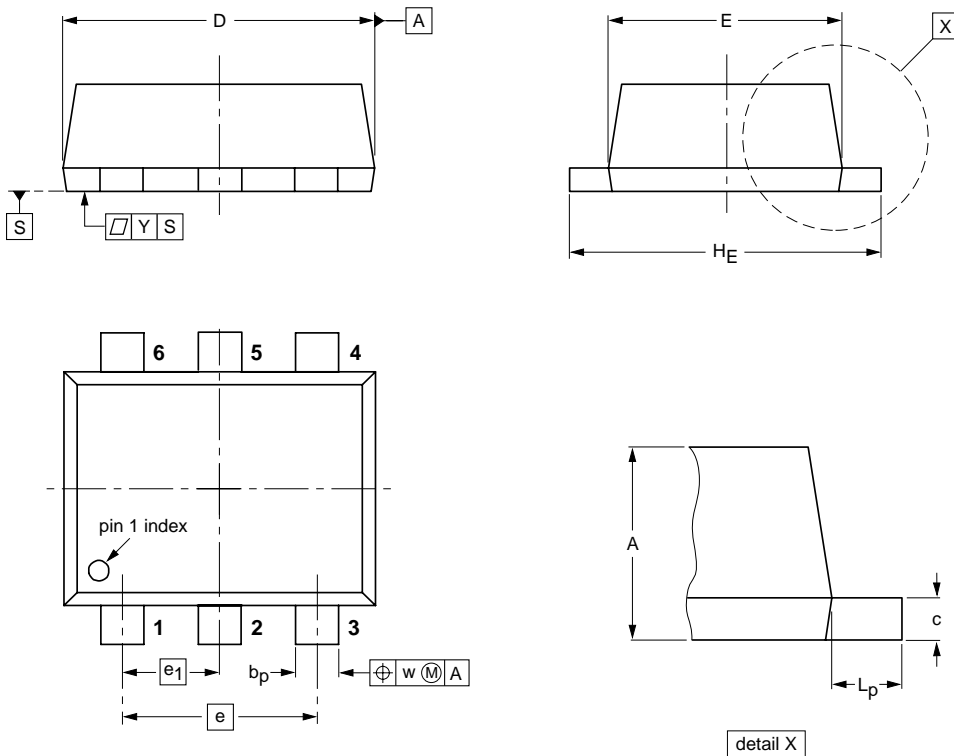
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PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT666



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

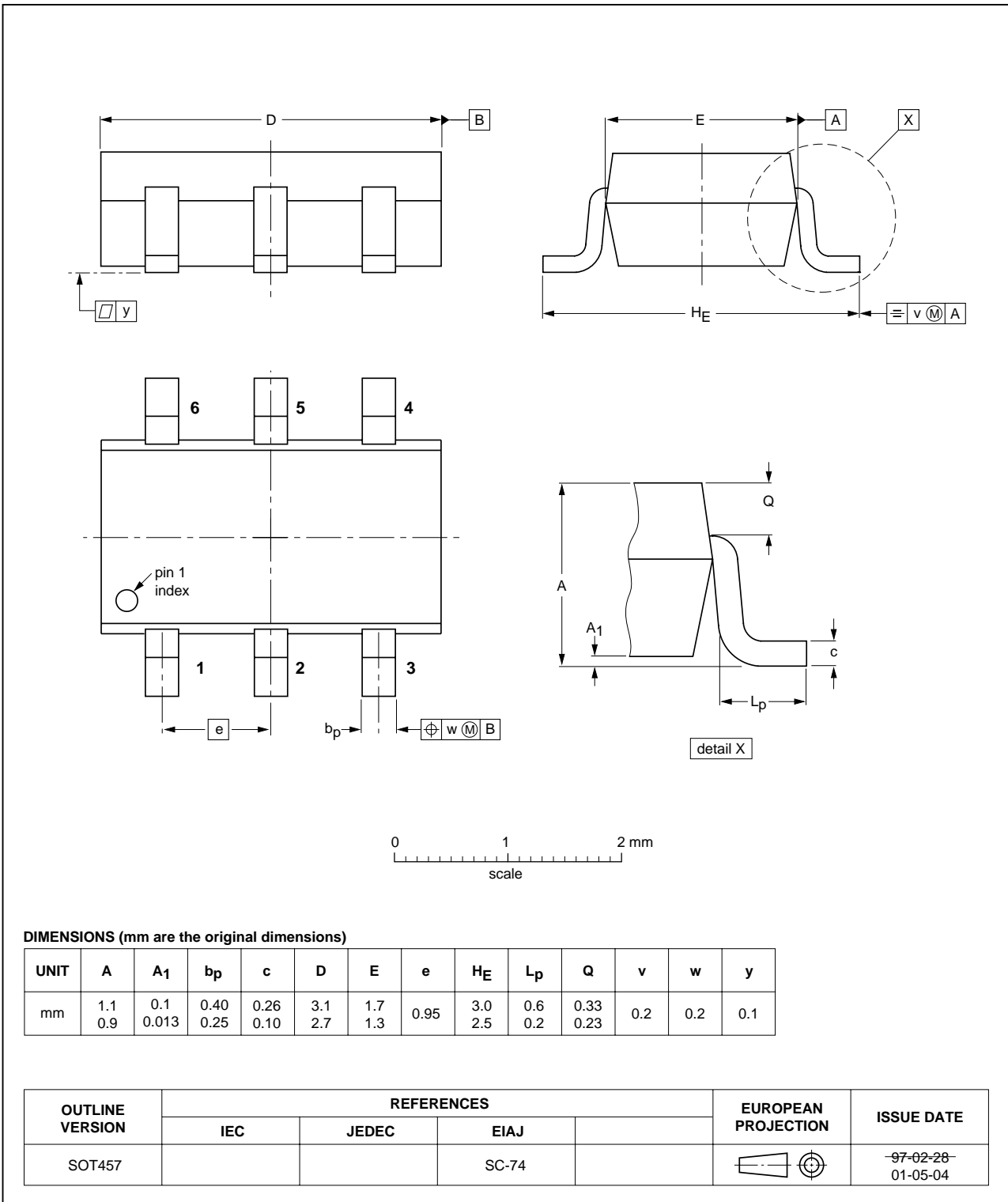
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT666					01-01-04 01-08-27

NPN/PNP resistor-equipped transistors;  
R1 = 22 kΩ, R2 = 22 kΩ

PEMD2; PIMD2; PUMD2

Plastic surface mounted package; 6 leads

SOT457

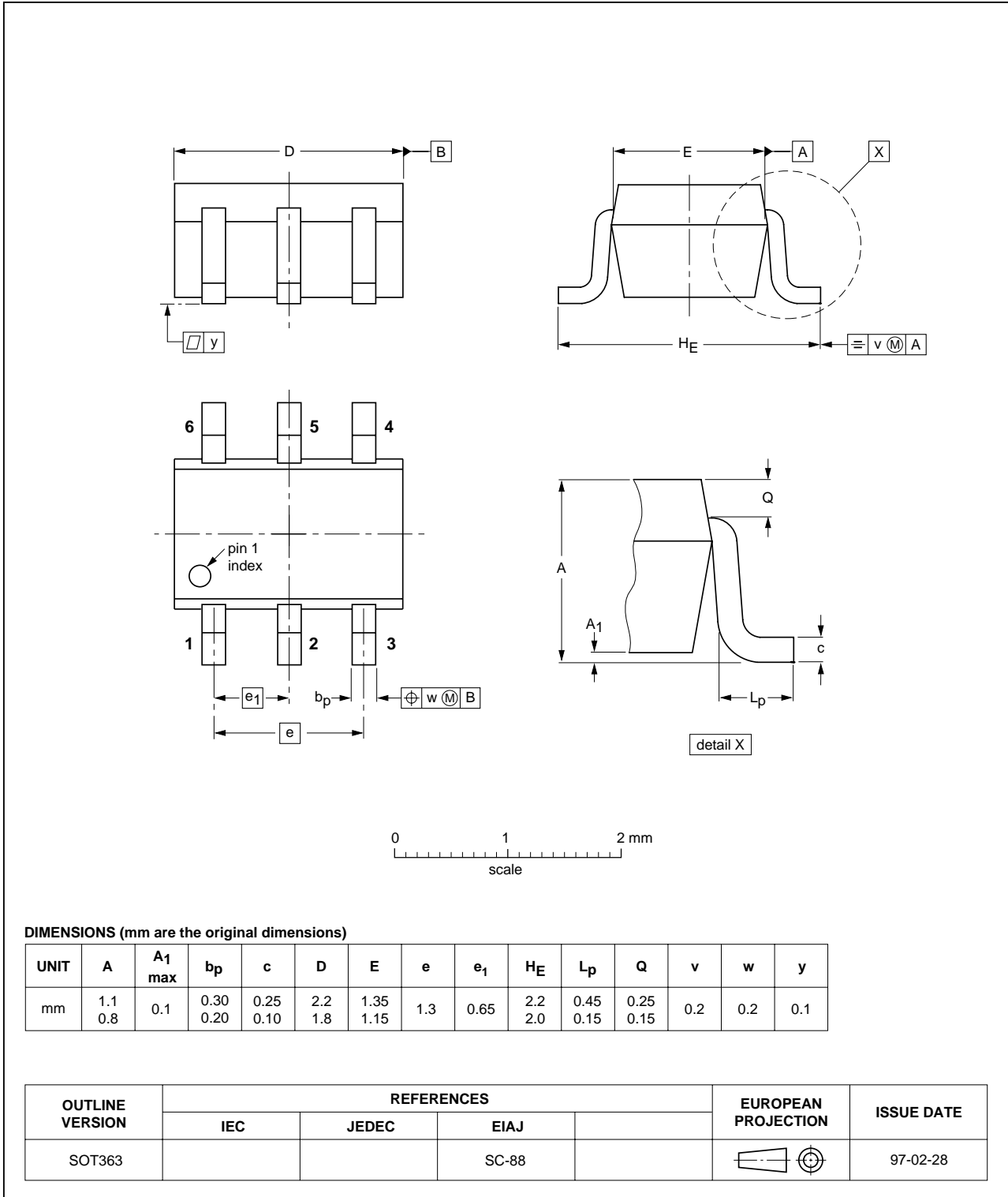


NPN/PNP resistor-equipped transistors;  
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SOT363





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#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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