SST4859 SERIES

Siliconix incorporated

T-35-25

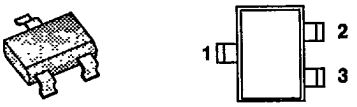
N-Channel JFET

The SST4859 Series is the surface mount equivalent of our 2N4859 device types. Its low cost and $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST4859	–10	25	5	2
SST4860	–6	40	5	3
SST4861	–4	60	5	4

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N4859 Series
- TO-92, See PN4091 Series
- Duals, See 2N5564 Series
- Chips, Order 2N485XCHP Series

PRODUCT MARKING	
SST4859	C59
SST4860	C60
SST4861	C61

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–30	V
Gate-Source Voltage	V_{GS}	–30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

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ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST4859		SST4860		SST4861		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	0.005		1		1		1	nA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-off Time	$t_{d(OFF)}$	SST4859 20 mA -10 V 464 Ω	8							
	t_f	SST4860 10 mA -6 V 953 Ω SST4861 5 mA -4 V 1910 Ω	5							

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

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